AN INNOVATIVE USE OF CURRENT MODE THRESHOLD FUNCTIONS FOR ENHANCED SWITCHING EFFICIENCY AND GATE DELAY

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ABSTRACT

Threshold logic functions are frequently implemented using current mode, a CMOS-based technique in which the sensor size affects the gate delay. The strength of the threshold gate design approach resides in the intrinsically complex functions that these gates implement. As a result, system realizations using threshold gates or lower gate levels than normal logic gates are possible. For better gate delay and switching energy, this study provides a novel implementation of current mode threshold functions. A mathematical technique is also suggested in order to quickly determine the sensor size that reduces the gate delay. The suggested current mode implementation approach consistently beats the present implementations in latency and switching energy, according to simulation findings on various gates designed using the ideal sensor size. The proposed architecture of this paper analysis the logic size, area and power consumption by using backend design.

Keywords: Current mode, operating speed,sensor sizing, threshold logic gates (TLGs).

INTRODUCTION

Gains in the performance of digital circuits due to parameter scaling that were exponential have disappeared. The capability of parallel processing can be increased by using additional technologies, like threshold logic gates (TLGs). A TLG is an N-input device that calculates the weighted sum of inputs. Current mode, the mono-stable to bi-stable transition logic element, neuron MOS, and single electron technology are a few examples of TLG designs. Several of these techniques are CMOS-based, allowing for the efficient synthesis of TLG-based circuits. TLGs are able to do complex logic operations and have more sophisticated logic processing than traditional Boolean gates. The essential elements of a TLG that determine a gate's operation are its weights. A basic TLG consists of N-inputs, a weight value for each input, and a threshold weight. The sum of the input weights is compared with the threshold weight. If it is greater thanthe threshold weight, then the digital output of TLG is logic high, and if it is less it will be logic zero. In the CMOS-based implementation considered in this paper, when the sum of the input weights is equal to thethreshold weight, then the gate is in undefined state. Weights are selected so that this case is avoided. The equation representing the output of a TLG is given as

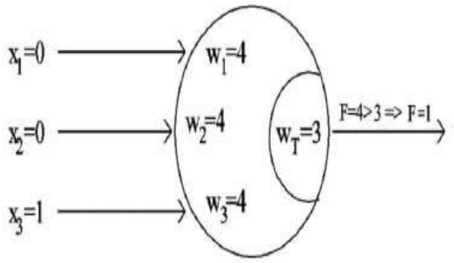


Fig. 1: Functionality of a TLG for a given weightconfiguration and input pattern.

We present a new implementation, which we call the dual clock current mode logic (DCCML), which results in both speed and switching energy [power-delay product (PDP)] improvements over the approaches. They consist of two parts: the differential part and the sensor part. All the p-MOS transistors in the sensor part have the same size S, which we call the sensor size. The sensor size impacts the performance ofall the three current mode implementations for any threshold logic function. It is a very time-consuming task to obtain the optimum sensor size through iterativeSPICE simulations, one simulation for a different sensor size. An automatic test pattern generation approach to detect delay defects in a circuit consisting of current mode threshold logic gates is introduced. Each generated pattern should excite the maximum propagation delay at the fault site. Manufactured weights may vary, and maximum delay is ensured by applying an appropriately generated set of patterns per fault. Experimental results show the efficiency of the proposed method. As an approach to clarifying the basic properties of threshold logic, the completely monotonic function is investigated. Its testing procedure, functional form, etc., are discussed by usinga new concept, mutual monotonicity. If the network contains cycles, however, the computation is not uniquely defined by the interconnection pattern and the temporal dimension must be considered. When the output of a unit is fed back to the same unit, we are dealing with a recursive computation without an explicit halting condition. We must define what weexpect from the network: is the fixed point of the recursive evaluation the desired result or one of the intermediate computations? To solve this problem we assume that every computation takes a certain amount of time at each node (for example a time unit).

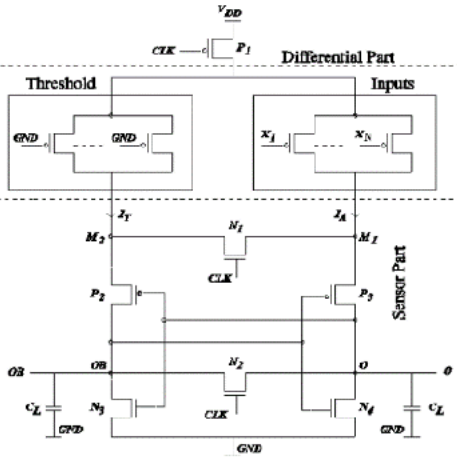


Fig. 2: Current mode TLG

Low-power dissipation is achieved by limiting the voltage swing on the interconnects and the internal nodes of the CMTL gates. High-performance is achieved by the use of transistor configurations that sense a small difference in current and set the differential outputs to the correct values. The realization of NAND, NOR, AND, OR logic gates and other logic functions using the CMTL gates is presented. We also present several implementations of CMTL gates and describe the relative advantages and limitations of these implementations. These computing elements are a generalization of the common logic gates used in conventional computing and, since they operate by comparing their total input with a threshold, this field of research is known as threshold logic.

LITERATUR SURVEY

Delay Analysis for Current Mode Threshold Logic Gate Designs. Current mode is a popular CMOS-based implementation of threshold logic functions, where the gate delay depends on the sensor size. This paper presents a new implementation of current mode threshold functions for improved gate delay and switching energy. An analytical method is also proposed in order to identify quickly the sensor sizethat minimizes the gate delay. Simulation results on different gates implemented using the optimum sensor size indicate that the proposed current modeimplementation method outperforms consistently theexisting implementations in delay as well as switching energy. Low power, high speed, charge recycling CMOS threshold logic gate A new implementation of a threshold gate basedon a capacitive input, charge recycling differential sense amplifier latch is presented. Simulation results indicate that the proposed structure has very low power dissipation and high operating speed, as well as robustness under process, temperature and supply voltage variations, and is therefore highly suitable as an element in digital integrated circuit design. A Low Power, High Performance Threshold Logic- Based Standard Cell Multiplier in 65 nm CMOS In this paper we describe the design, simulation, fabrication, and test of a 32-bit 2's complement integer multiplier constructed from a combination of CMOS standard cells and threshold logic elements in a 65 nm low power process. As compared to a multiplier designed solely using CMOS standard cells, the threshold logic based multiplier Is 1.23x smaller and consumes 1.41x less dynamic power and 2.5x less leakage power at the same process corner.

Current-Mode Threshold Logic Gates(CMTLG).

Fig. 2 shows the a general circuit diagram of the CMTL gates. The low-swing inputs are fed to a PMOS based CMTL gate. The CMTL gate senses the lowinput swings, performs the logic computations and creates full-swing output voltages. The output nodes of the CMTL gate with full-swing are used as inputs tothe nMOS based interconnect driver. In the next section, we describe the current-mode threshold logic gates and present several implementations of threshold logic gates. A threshold gate is a super-set of logic gates such as AND, NAND, OR, NOR. It can be used to realize more complicated functions such as majority function in a single logic gate. Fig. 3. shows the basic operation of the current-mode threshold logic gate. Since the input voltage swing is between VL and Gnd, the PMOS transistor is used to translate the input voltage into current. When the input at the gate terminal of the PMOS transistor is Gnd it can drive a larger current compared to the PMOS transistor with the a gate input voltage of VL. For small values of VL, the PMOStransistor is always ON.

CMTLG AND DCML IMPLEMENTATIONS OF ATHRESHOLD LOGIC FUNCTION

The nodes connecting the differential part and the sensor part on the input side and the threshold side are M1 and M2, respectively. The sensor part has three p- MOS transistors P1, P2, P3, and four n-MOS transistors N1, N2, N3, and N4 as shown in figurebelow. If the size of the sensor is S, then all the p-MOStransistors in the sensor part have S μm size and all the n-MOS transistors in the sensor part have a size smallerthan S μm. The operation of the CMTLG is divided into two phases: the equalization phase and the evaluation phase. These phases are explained with the help of Figs. 1. and 5. When the applied clock (clk) to the CMTLG is high, then the circuit is in the equalization phase. When clk is low, then the circuit is in the evaluation phase. In the equalization phase, transistors N1 and N2 are ON, nodes M1 and M2 have the same voltage because of transistor N1, and nodes O and OB have the same voltage because of transistor N2 (see also Fig. 1). In the evaluation phase, transistors N1 and N2 are OFF, and if the threshold current is less than theactive current, then the voltage at node O rises faster than that at node OB. If during the evaluation phase the threshold current exceeds the active current, then the voltage at node OB rises faster than that at node O. Fig. 5 shows the two phases of clock, the voltage at the output nodes O and OB, and the voltage difference between the output nodes O and OB (dV).

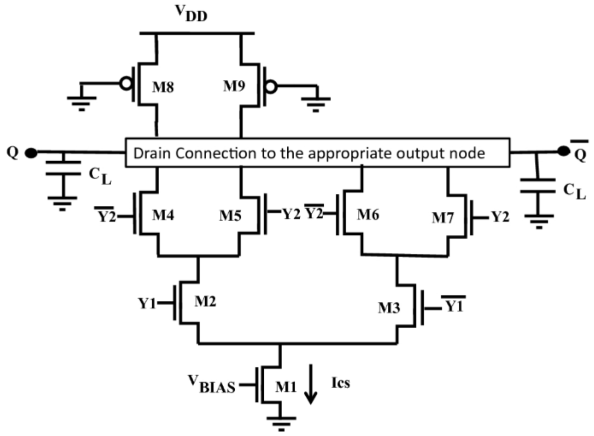


Fig. 3: Block diagram of differential current modelogic.

An alternative differential clock threshold logic implementation is presented in, and it is referred to as the differential current mode logic (DCML) approach. Its block diagram is shown in Fig. 3.4. It is also dividedinto the differential part and the sensor part. The currents through the threshold part and the inputs part are also denoted by IT and IA, respectively. The sensorpart consists of four p-MOS transistors, labeled P1–P4, and six nMOS transistors, labeled N1–N6. The load capacitance CL is applied to both the output nodes O and OB.

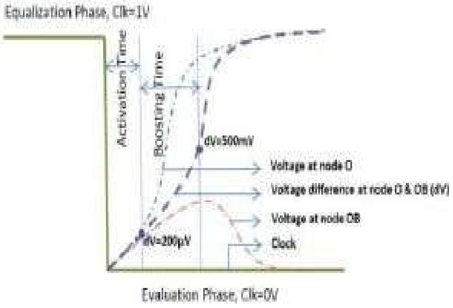


Fig. 5: Output voltages and their difference in the twoclock phases for DCML.

The applied clock is divided into two phases: when the clock is high the TLG is in the equalization phase and when it is low it operates on the evaluation phase. In the equalization phase, nMOS transistors N1, N2, N3, and N6 are active. Transistor N1 equalizes the voltage at nodes M1 and M2. Similarly, transistor N2 equalizesthe voltage at nodes M3 and M4.Demerits of Existing System. Existing system consist of two parts: the differential part and the sensor part. All the pMOS transistors in the sensor part have the same size S, which we call the sensor size. The sensor size impacts the performance of all the three current mode implementations for any threshold logic function. It is avery time-consuming task to obtain the optimum sensorsize for different sensor size, which is the drawback. In the proposed we are reducing the power.

LOW POWER AND HIGH-SPEED DUAL- CLOCK-BASED CURRENT MODE TL IMPLEMENTATION.

A new TLG implementation is proposed. It is called DCCML. As the name indicates, two clocks are used to achieve low power consumption and high speed. The block diagram DCCML is shown in Fig.

4.1. As in previous approaches, the DCCML is divided into two basic blocks: the differential block and the sensor block. The differential block is further divided into four blocks: the positive threshold, the negative inputs, the negative threshold, and the positive inputs. All the transistors in the differential block are equal-sized pMOS transistors and are connected in parallel, as shown in Fig. 6. The sensor block consists of six pMOS transistors P1 ··· P6 and three nMOS transistors N1, N2, and N3. The gates of transistors P1 and N1 are connected to Clk1 and the gates of transistors P2, P5, and P6 are connected to Clk2. Transistor N1 acts as an equalizing transistor and it equalizes the voltage at nodes OP and OPB. Transistors P5 and P6 isolate the differential block from the sensor block. The transistors in the positive threshold and negative threshold are always active. Transistors in the positive and negative inputs blocks are active depending upon the input pattern applied. The input pattern applied for the positive inputs block is denoted by {x1, x2,..., xI . Let N denote the number of inputs, and I denote the number of positive inputs. Then the number of negativeinputs is N–I. The input pattern applied for the negativeinputs block is denoted by {xI+1, xI+2,..., xN . Consider a function f, with a possible weight configuration {w1,w2 : wT ,w3, w4}={2, 2:3, −1, −1}. In the given weight configuration, we have two positive weights w1andw2 and two negative weights w3 and w4. Weights w1 and w2 are implemented in the positive inputs section and weights w3 and w4 are implemented in the negative inputs section. Thethreshold weight wT is implemented in the positive threshold section. The current through the four blocks (positive threshold, negative inputs, negative threshold,and positive inputs) are denoted by IPT , IN I , INT , and IP I , respectively. The currents through transistors P5 and P6 are denoted by I 5 P and I 6 P. Here, I 5 P = IPT + IN I and I 6 P = INT + IP I . Nodes OP and OPB

are the output nodes. The load capacitance is denoted by CL. The operation is divided into three phases: the equalization phase, the pre-evaluation phase, and the final-evaluation phase. When clocks Clk1 and Clk2 are high, then the circuit is in the equalization phase. Whenclocks Clk1 and Clk2 are low, then the circuit is in the pre-evaluation phase. It is noted that when the twoclocks are not completely aligned the operation of the gate is not effected. The possible cases of misalignmentare: 1) the falling edge of Clk2 comes before the fallingedge of Clk1 and 2) the falling edge of Clk2 comesafter the falling edge of Clk1 [13]. In the first case, the current from the differential part is equalized because of transistor N1 and the evaluation phase starts after thefalling edge of Clk1. In the second case, there will beno current from the differential part as Clk2 is notactive yet. Hence, the pre-evaluation phase starts after the falling edge of Clk2. The implementation avoids a very early arrival of Clk1. In that case, a non- stable signal might result in erroneous output.

If the current I 6 P through the pMOS transistor P6 is greater than the current I 5 P through the pMOS transistor P5, then the voltage at the output node O P rises faster than the output node OPB. As a result, high voltage is obtained at output node O P and low voltage occurs at output node OPB. Otherwise, the voltage at the output node OPB rises faster than the output node O P. As a result, high voltage is obtainedat the output node OPB and low voltage is obtained at node O P. In DCCML, the pMOS transistors P1, P2, P5, P6 and the pMOS transistors in the differential block are used to provide the initial voltage at the output nodes O P and OPB. Using Clk2, we restrict the current flow from the differential block to the sensor block, once initial voltage difference is established at the nodes OP and OPB; in this way we stop the current flowing from the differential block to the sensor block. Using Clk2, we are able to minimize power consumption in the circuit. Transistors P5 and P6 are also used to isolate high capacitance circuit block (the differential block) at the output nodes. Hence, in the final evaluation phase the sensor block drives the load capacitance as well as the capacitance from a single transistor P5 or P6. Delay is reduced because the duration of the final evaluation phase is small. The voltage at the output nodes O P and OPB and thevoltage difference (dV) at the output nodes O P and OPB are shown in Fig. 4.3 for the three clock phases.In particular, the delay of the DCCML is divided into two time phases: the activation time and the boosting time. The activation time is the time taken by the circuit to develop an initial voltage difference at then output nodes O P and OPB. The boosting time is the time taken by the DCCML to bring the initial voltageto the correct voltage at the output nodes O P and OPB.In the pre-evaluation phase, both the differential part and the sensor part are active, and therefore the activation time is not affected. In the final evaluation phase, the differential part is kept inactive using Clk2. Therefore, the effect of internal capacitance due to the differential part is isolated. Hence, it takes very little time to boost the outputs to the final value. The power is also reduced due to the isolation of the differential part.

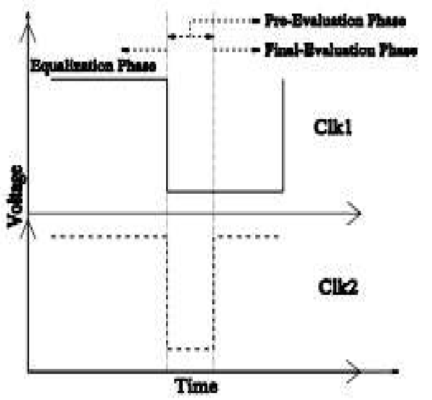


Fig. 7. Clocks in DCCML.

DELAY MINIMIZATION BY AN APPROPRIATE SENSOR SIZE SELECTION.

This section presents an analytical formula to compute the sensor size that minimizes the gate delay. Let N denote the number of inputs, N the sum of all positive input weights, and T the sum of the threshold weight and negative input weights. Our analysis assumes that all the input weights areconnected in parallel, and that each weight wi can be implemented by wi unit width pMOS transistors connected in parallel. This is an accurate assumption. We have implemented TLG weights using a smaller number of wider pMOS transistors connected in parallel and SPICE simulations showed no difference in the performance of the TLG. This is further explained in the example below.

Example 2: Consider a threshold function where N, the sum of positive input weights, is 11. Let also T, the sum of the threshold weight and negative input weights, be 4. In this function, we have (N, T) = (11, 4). Gates {11:4}, {6, 5: 4}, {5, 5, 1: 4}, {5, 4, 1, 1: 4},
{4, 4, 1, 1, 1: 4}, and {1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1: 4}
were implemented in the 45-nm technology. SPICE simulation shows an identical delay of 297 ps. In the following, we will not differentiate among functions for which the sum of all positive input weights is N, and the sum of the negative input weight and threshold weight is T . Since all these threshold functions exhibit the same delay, these functions will be denoted by the pair (N, T). The remaining focus is on how to determine the optimum sensor that minimizes the delayof any (N, T) function. The proposed method considersthat the TLG operates under an input pattern that exhibits the worst case propagation delay, and thenfocuses on deriving an analytical model that expresses TLG delay in terms of the sensor size S in that setting. In a first step, we identify the pattern that gives the highest delay for the function. In a second step, we consider this worst case scenario, and the delay will be expressed as a function of the sensor size S. Then, we operate on that function in order to optimize the sensor size S. In the first step, it is shown that when T +1 inputs are active then the TLG exhibits its worst delay. Let NA = i wi , such that xi = 1. Such inputs i are called active, and the respective pMOS transistors are also called active. Assume that the initial current flowing through an active minimum-sized pMOS is Ip. Then the current flowing through the threshold side of the TLG is T · Ip, and the current flowing through the input side for NA inputs being active is NA · Ip. To obtain the worst case delay for logic 1 at the output node O, the current difference IA−IT should be minimum. For logic 0, this current difference should also be minimum. Since transistors on the threshold side are always ON, the maximum delay for a rising transition of the output is obtained when we have T +1 active transistors. Likewise, T −1 active transistors tendto obtain the worst case delay for a falling transition at the output. However, it is known that the worst case delay occurs for rising output transition [1]. Hence, a worst case delay pattern is one that gives the leastcurrent difference at nodes M1 and M2. The following is an example where SPICE simulations confirm this analysis.

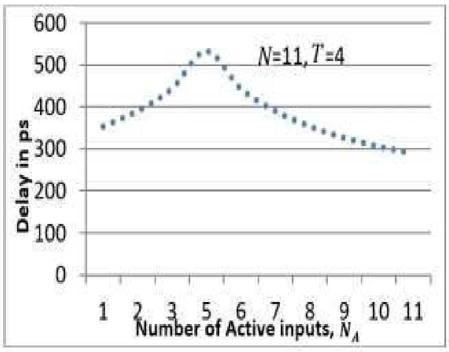
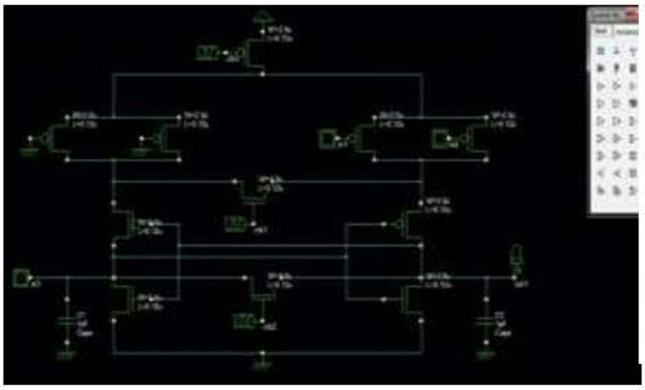


Fig. 9. CMTLG delay with N = 11 and T = 4 as NA varies.

RESULT

Current mode TLG.Schematic.



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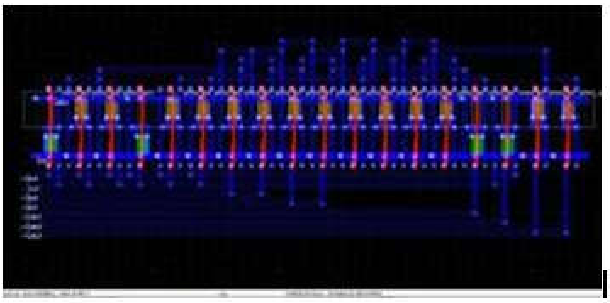
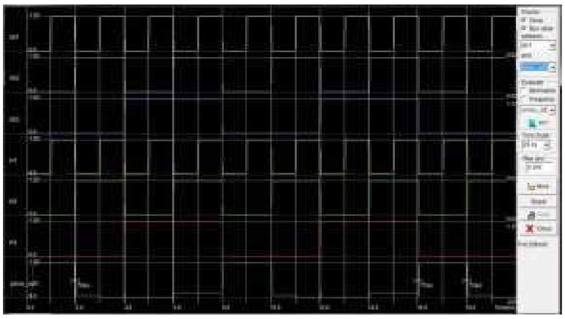
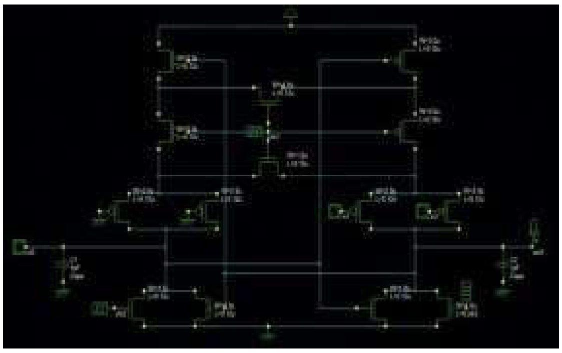


Simulation.



Differential current mode logic.Schematic.



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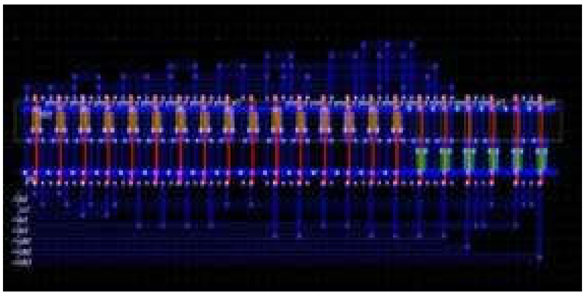

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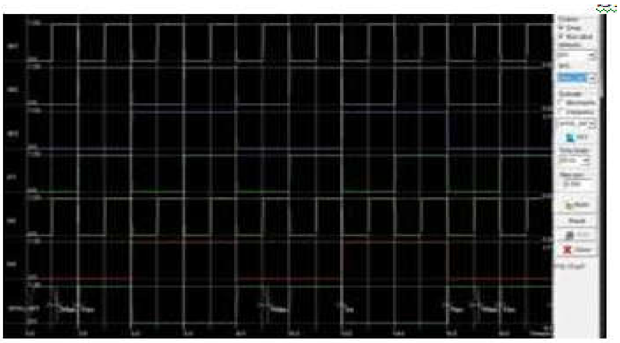
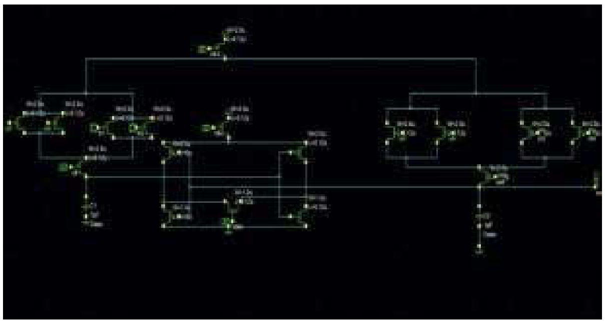


Schematic of DCCML TLG.



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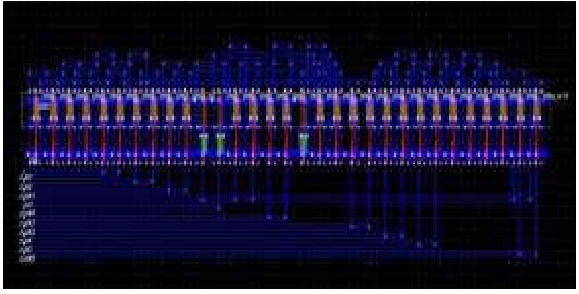

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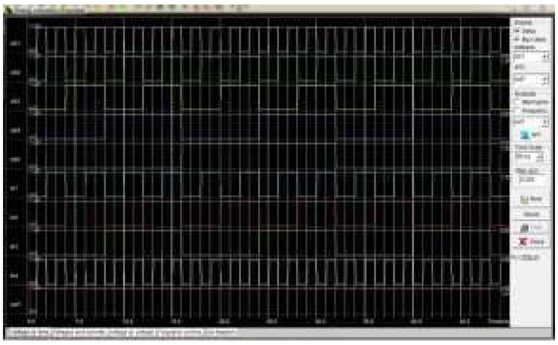

CONCLUSION

An analytical method has been proposed to identify quickly the transistor size in the sensor component of a current mode implementation that ensures very low gate delay (very close to theminimum), independent of the current mode method used to implement the threshold logic function. A new current mode implementation method was also proposed that outperforms existing implementations both in gate delay as well as energy.

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