ASSYMMETRIC MULTILEVEL INVERTER ANALYSIS FOR RESISTIVE LOADS WITH REDUCED SWITCH COUNT

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ABSTRACT
Higher voltage levels have been attained by using multiple inverters. Asymmetric MLI and symmetric MLI are the two different types of multilevel inverters used in cascaded multilevel inverters. By utilizing bidirectional switches and a DC supply, a symmetric multilayer inverter raises the output voltage level. In asymmetric MLI, switching capacitor units are used in place of DC sources. While utilizing a maximum number of switches with a high total harmonic distortion, the number of output levels achieved in the symmetric arrangement is lower since each and every input DC source has the same value (THD). Different amounts of voltage can be achieved because asymmetric MLI input DC sources are not the same. By adding such different levels of voltage more levels can be obtained with less number of devices with consequent reduction in THD. The multilevel inverter topologies with low total harmonic distortion, less number of switches and increased output voltage levels are to be obtained. The voltages and THD are to be analyzed by using MATLAB- SIMULINK R2016a

INTRODUCTION
The power sector has shown a great deal of interest in multilevel inverters. The general purpose of a multilayer inverter is to create a sinusoidal voltage out of a variety of voltage levels [1]. Three different multilevel topologies exist. Multilevel inverters include cascaded MLI with independent DC sources, flying capacitor MLI, and diode clamped MLI. An array of switches, capacitors, and voltage sources are found in multilevel inverters. The power switch must only endure low voltage whereas the switches allow the addition of capacitor voltages, which reach high voltage at the output. The created output waveform adds additional steps as the number of levels rises, creating a stair case wave pattern that will eventually approach sinusoidal with the least amount of harmonic distortion. [2] – [6].
The cascaded MLI are used in asymmetric and symmetric types. In the symmetric configuration, a novel stair-case modulation technique with the cascaded hybridized MLI in single phase. The value of the each and every input DC source are same, because of this criteria the number of output levels obtained are less inspite of using more number of switches with high total harmonic distortion(THD) [7]. In attaining higher levels of voltages and power levels, cascaded MLIs are more flexible. Its property is used to achieve the magnitude of power from the inverter. These Cascaded MLIs are made by joining the respective H-bridge multilevel inverters series output terminals [8], [9]. Hence, this topology is helpful in achieving higher levels of power by using small power, voltage rating devices in multilevel inverters. Due to its property if fault has occurred in any one of the single cells of inverter, the fault found rapidly and easily replaced. In case of fault in any of the inverter cell, in order to achieve continuity in theoutput of the inverter [10]. A flexible control technique must be used to divert the cell which is faulty without interfering with the load [11], [12]. With the improvements in MLI, there is a necessity for the novel designing ofmodulation techniques for achieving the high quality output. Hence, many modulation strategies have been found based on converter configuration. The pulse width modulation scheme is highly suitable for cascaded hybrid MLI. It produces high quality output waveform. Incontrast, Asymmetric MLI with switched capacitor unit. The value of input DC sources are not same because of which different levels of voltages are obtained. By combining such voltage levels more levels are produced with a fewer number of switches and low THD [13].

SYMMETRIC HYBRIDIZED CASCADED MLI TOPOLOGY
The circuit diagram of 5-level symmetric multilevel inverter shown in Fig.1. The hybridized cascaded H-

bridge configuration is used as in simulating the 5-level symmetric MLI which is presented in Fig.1. Five level symmetricmultilevel inverter operation can be analyzed in 2-stages.
In stage-1, +1V, 0V, -1V are the output levels. In stage-2
+2V, 0V, -2V are the output levels. The output levels are given by the interconnection of bidirectional switch to the leg-2.

Table 1 Five level symmetric MLI parameters

Item	5 level Symmetric MLI
DC sources(0-30V)	2
Switches (MOSFET)	5
Diodes	0
Capacitors (100 μF)	0
R-load (50Ω, 100Ω)	1

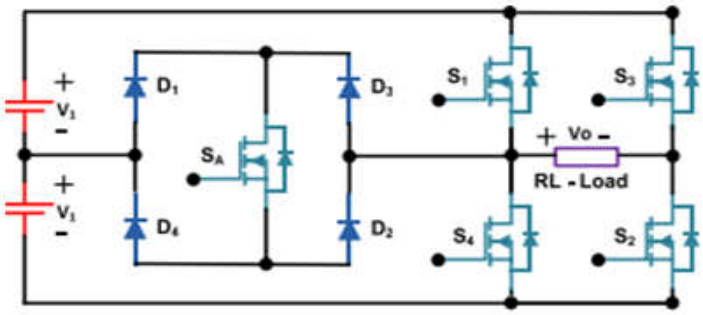


Fig.1 circuit diagram of 5-level symmetric multilevel inverter

Table 2 Switching sequence of 5-level symmetric multilevel inverter.

Output voltage levels	Switching States				
Switches	S_1	S_2	S_3	S_4	S_A
+2 V	1	1	0	0	0
+1 V	0	1	0	0	1
0 V	0	1	0	1	0
0 V	1	0	1	0	0
-1 V	0	0	1	0	1
-2 V	0	0	1	1	0

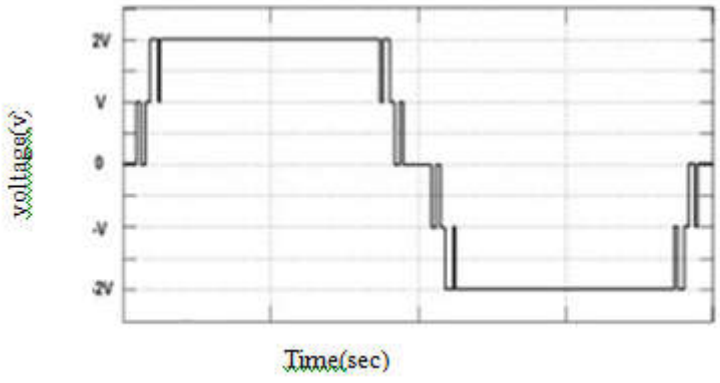


Fig.2. Output voltage waveform of 5-level symmetric multilevel inverter.

In the symmetric hybridized and asymmetric switched capacitor MLI, different magnitude of DC sources are utilized. Number of devices are utilized in increasing the number of output levels. Table 1 shows five level symmetric MLI parameters. Table 2 shows the switching sequence of 5-level symmetric multilevel inverter. Fig.2. shows output voltage waveform of 5-level symmetric MLI. In the symmetric MLI same magnitude of input dc sources are used.

ASYMMETRIC SWITCHED CAPACITOR MLITOPOLOGY

Fig.3(a) shows circuit diagram of 5-level asymmetric switched capacitor MLI. The asymmetric switched capacitor consists of battery, switched capacitor, 2 switching devices and diode. Input voltage is doubled by the capacitor at the load terminal [14] – [16]. Input voltage is given to the circuit, switch S1 is used in discharging the capacitor. Switch S2 is used in charging the capacitor. At the load side V and 2V output voltages are produced by theasymmetric MLI with fewer number of switches.

Table 3 Five level Asymmetric MLI parameters

Item	5 level Asymmetric MLI
DC sources (0-30V)	1
Switches (MOSFET)	2
Diodes	1
Capacitors (100 µF)	1
R-load (50Ω, 100Ω)	1

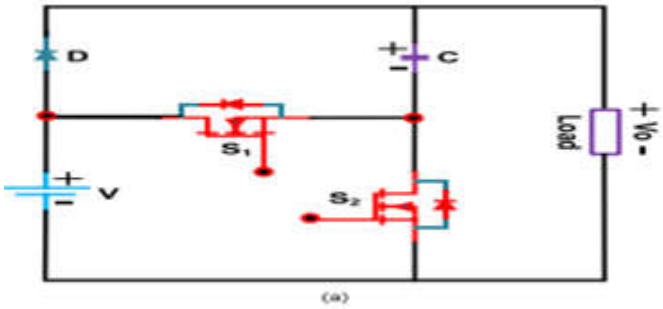


Fig.3(a)

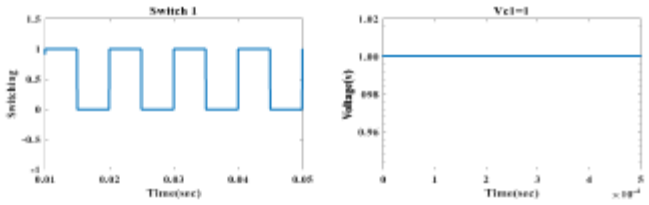


Fig.3(a) Circuit diagram of 5-level asymmetric MLI.

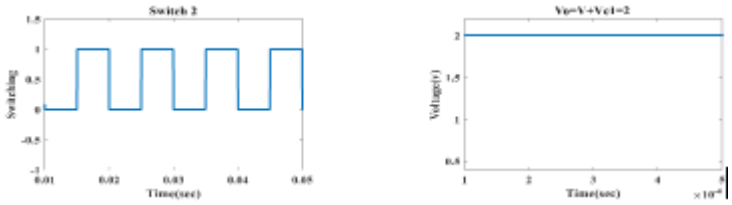


Fig.3(b) Output voltage waveform of 5-level asymmetric MLI.

Table 3 shows five level asymmetric MLI parameters. Switching sequence of S1 and S2 during ON & OFF time along with output voltage shown in fig. 3(b).

During charging time, the input voltage is same as load voltage. The capacitor charges to a voltage of 1V. During discharging of the capacitor input voltage is added to capacitor voltage and the output voltage is doubled. Hence load voltage is 2V. In asymmetric switched capacitor configuration less input voltage gives more output voltage for multilevel inverters.

Table 4 Seventeen level asymmetric MLI parameters

Item	17 level Asymmetric MLI
DC sources (0-30V)	2

Switches (MOSFET)	10
Diodes	2
Capacitors (100 µF)	2
R-load (50Ω, 100Ω)	1

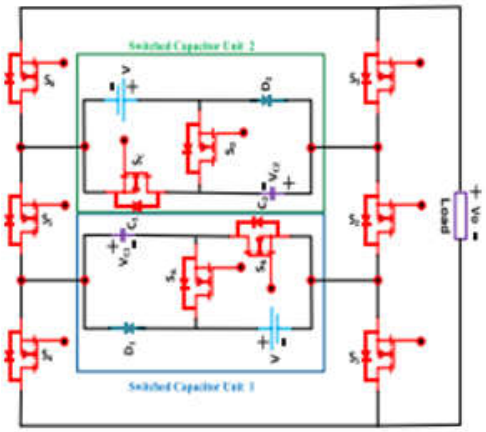


Fig.4 Circuit diagram of 17-level asymmetric multilevel inverter.

Fig.4 shows circuit diagram of 17-level asymmetric multilevel inverter.17-level asymmetric configuration consists of 10 switches, 2 diodes, 2 switched capacitor unit, 2 batteries and 2 capacitors. Table 4 shows seventeen level asymmetric MLI parameters. The 17-level asymmetric MLI gives peak voltage of 100 V at the load side. Individual pulses are produced by switched capacitor unit. The output voltage is obtained by combining all the individual unit voltages.

RESULTS OF SIMULATION

The staircase pulse width modulation scheme is used to produce pulses of symmetric hybridized cascaded MLI and asymmetric switched capacitor MLI are implemented inMATLAB Simulink R2016a.

Table 5 Switching sequence table of 17 level asymmetric MLI

V_O Level	S_1	S_2	S_3	S_4	S_5	S_6	S_A	S_B	S_C	S_D	Output voltage level expression	Output Voltage (V)
1	1	0	1	0	1	0	1	0	0	1	$4V+V_{C1}+V_{C2}$	100
2	1	0	1	0	1	0	0	1	0	1	$4V+V_{C2}$	87.5
3	0	0	1	1	1	0	0	1	1	1	$3V+V_{C2}$	75
4	1	0	1	0	1	0	1	0	1	0	$4V+V_{C1}$	62.5
5	1	0	1	0	1	0	0	1	1	0	4V	50
6	0	0	1	1	1	0	0	1	1	0	3V	37.5
7	1	0	0	0	1	1	1	0	0	0	$V+V_{C1}$	25
8	1	0	0	0	1	1	0	1	0	0	V	12.5
9	1	1	1	0	0	0	0	1	1	0	0	0
10	0	1	1	1	0	0	0	1	0	0	$-V_1$	-12.5
11	0	1	1	1	0	0	1	0	1	0	$-V-V_{C1}$	-25
12	1	1	0	0	0	1	0	1	1	0	-3V	-37.5
13	0	1	0	1	0	1	0	1	1	0	-4V	-50
14	0	1	0	1	0	1	1	0	1	0	$-4V-V_{C1}$	-62.5
15	1	1	0	0	0	1	0	1	0	1	$-3V-V_{C2}$	-75
16	0	1	0	1	0	1	0	1	0	1	$-4V-V_{C2}$	-87.5
17	0	1	0	1	0	1	1	0	0	1	$-4V-V_{C1}-V_{C2}$	-100

The results are compared with resistive loads. Table 5shows the switching sequence of 17-level asymmetric MLI.

SYMMETRIC HYBRIDESED CASCADEDMULTILEVEL INVERTER

The simulation of MLI operated with resistive load for 100 V output voltage, one ampere output current is obtained. The Rms value of output voltage and current obtained are

67.2 V and 1.404 A respectively. Fig.5 Shows output current, output voltage and individual output voltage waveforms of 17-level symmetric multilevel inverter.

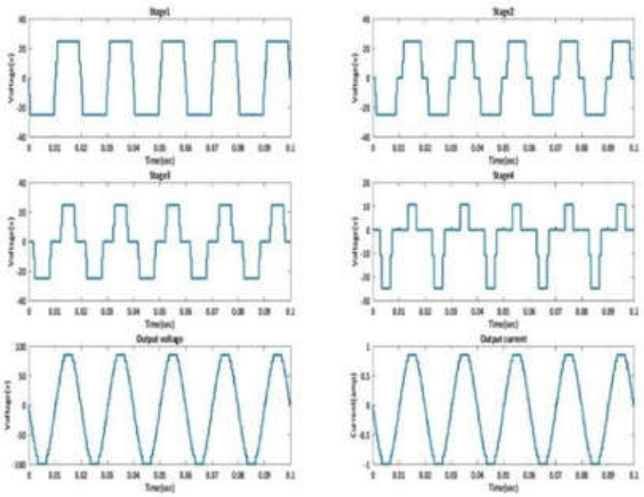


Fig.5 Output current, output voltage and individual output voltagewaveforms of 17-level symmetric multilevel inverter.

In 17-level symmetric multilevel inverter, pulses are generated individually as stage -1, stage-2, stage -3 and stage-4. Finally, total output voltage is obtained bycombining all the individual stage voltages.

ASYMMETRIC SWITCHED CAPACITORMULTILEVEL INVERTER

The simulation of MLI operated with resistive load with 100V of the peak output voltage. The Rms value of output current and voltage obtained are 1.06 A and 72.71 respectively.

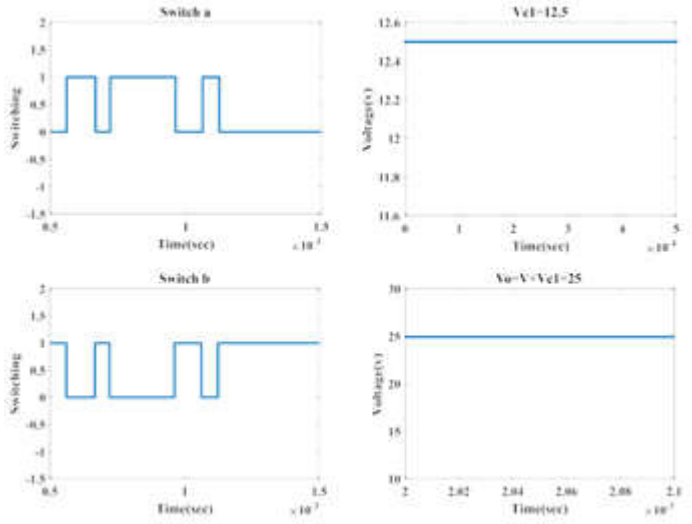
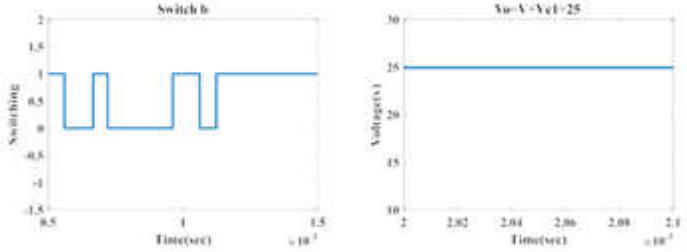


Fig.6(a)



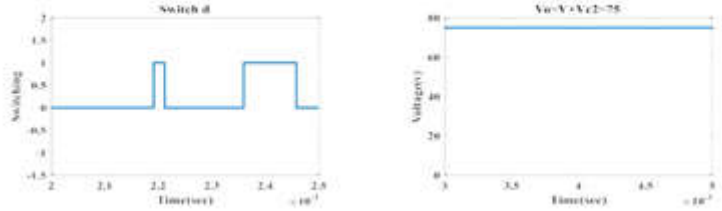


Fig.6(b)

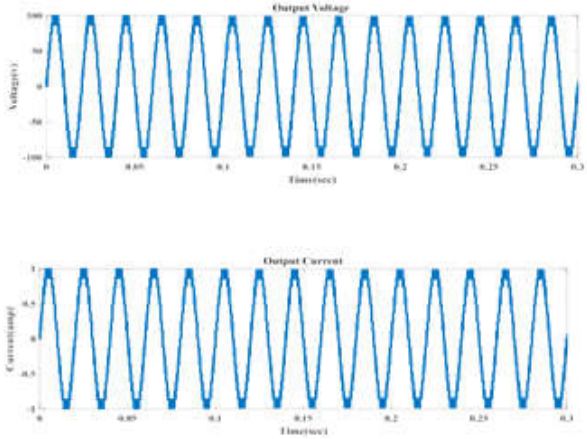


Fig. 6(c)

Fig.6(a) 17 level MLI capacitor unit-1 waveform Fig.6(b). 17 level MLI capacitor unit-2 waveform. Fig.6(c). 17-level MLI output current and output voltage waveforms.

Figures.6(a), 6(b) &6(c) shows the waveforms of switched capacitor unit-1, unit-2 and output current and output voltage of 17-level asymmetric MLI. In asymmetric multilevel inverter, pulses are generated individually as switched capacitor unit-1 and switched capacitor unit-2. In switched capacitor unit-1 output voltage is 25V. In switched capacitor unit-2 output voltage is 75. The total output voltage is obtained by combining capacitor unit-1 and capacitor unit-2. The total output voltage is 100V. Fig.7 Shows output voltage waveform of asymmetric switched capacitor MLI and its corresponding harmonic spectra.

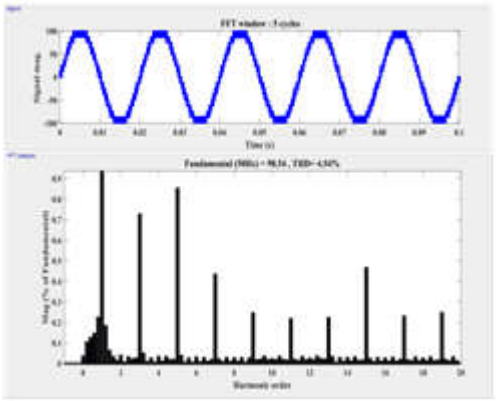


Fig.7 Output voltage waveform of asymmetric switched capacitor MLI and its corresponding harmonic spectra

Table 6 Simulation output results

Type of inverter configuration	Type of Load	Output peak-peak voltage (Volts)	Output peak-peak voltage (Volts)	Output peak-peak current (Amps)	Output RMS current (Amps)	Frequency (Hz)	THD (%)
17-level Symmetric	R-load	200	67.92	2	1.414	50	5.41
17-level Asymmetric	R-load	200	72.72	2	1.06	50	4.54

Table 6 shows simulation output results.

CONCLUSION

The multilevel inverter topologies to achieve high output voltages with fewer number of switches and low THD are obtained with the proposed scheme. In case A, simulation has been carried out for the resistive load and THD with 17 level symmetric MLI were presented. In 17-level asymmetric multilevel inverter gives 5.41% THD. In case B, 17 level asymmetric switched capacitor multilevel inverter a THD with 4.54% has been achieved. It is inferred that by using a fewer number of switches and less number of batteries also low THD is obtained along with the high quality output voltage.

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