A cascaded multilevel inverter that is based on a single-phase PV system with boost DC-link integration

[1]T.Karthik, [2]T.Karthik, [3]P.Sujarella, [4]V.Naresh
[1,2,3]Assistant Professor, [4]UG Student, [1,2,3,4]Department of Electrical and Electronics Engineering,
Visvesvaraya College of Engineering & Technology, Hyderabad, India.

ABSTRACT

In this work, a cascaded multilevel inverter with boost DC-link integration that is based on a single-phase PV system is described. The BDIMLI is realized by coupling two two-level boost DC-link converters (TBDCs) with a hybrid H-bridge inverter and using symmetrical voltage sources. For typical cascaded multilevel inverters, several discrete DC source and circuit components are required. On the other hand, switched capacitor multilevel inverter topologies require fewer sources and components but larger capacitors. The suggested TBDC units employ lower capacitance and component counts overall by charging the capacitors to the proper voltage with a high switching frequency. Without changing any of the circuit's components, the suggested topology can create 9-, 11-, and 13-level outputs with the right selection of capacitor voltage levels. Besides, the proposed topology produces low-frequency common-mode voltage. The comprehensive analysis of BDIMLI in comparison with recent multilevel inverter topologies is presented. An experimental prototype of BDIMLI is built and its dynamic behavior with different load conditions is presented for both 9- and 13-level operations.

INTRODUCTION

The need for multilayer inverters has significantly increased in each field of electrical engineering, including grid-connected renewable energy systems, electric vehicles, electric drives, etc (MLIs). In addition to having a higher output voltage than conventional two-level inverters, MLIs also have lower common-mode voltage (CMV), smaller filters, lower switching frequency, and decreased dv/dt [1]. MLI topologies are frequently split into three categories: flying capacitors MLI (FCMLI), neutral-point clamped MLI (NPCMLI), and cascaded H-bridge MLI (CHBMLI) [4, 5]. Electric motors and other power quality-related industries employ these MLIs because of their outstanding performance. The NPCMLI and FCMLI topologies require large amounts of diodes, capacitors, and rectification circuits to address voltage imbalance, whereas the CHBMLI topologies call for a large number of isolated voltage sources. Consequently, it results in higher costs and worse efficiency. A few MLI topologies are reported with reduced switch count and voltage sources [6–11] to improve compactnessand efficiency. New pulse-width modulation (PWM) techniques [9] are presented to maintain constant CMV and reduce leakage currents in cascaded half-bridge MLI topologies. Also, fault-tolerant methods [10] are incorporated for reduced switch count SCMLI (RSCMLI). However, none ofthese topologies offers high gain boost factor, which is essential in renewable energy applications.In recent times, several boost derived MLIs are reported using boost converter [12], Z-source network [13, 14], coupled inductor [15] and switched capacitor (SC) [16–18] techniques. Z- source network and coupled inductor-based step-up MLIs provide high voltage gains owing to high switching stress and losses, while SCMLI topologies provide high efficiencies but require large capacitor size and switch count. SC cell comprised CHBMLI [16] with low capacitor size isproposed for high-frequency applications. Further, similar structures with large capacitor size for power frequency applications are adopted. The SCMLI topologies presented in [16] use parallel charging and series discharging of the capacitor. Hence the size of the capacitor is a function of frequency and load resistance. Modified H-bridge based SCMLI topologies similar to [9] are reported to further reduce the switch count. These SCMLI topologies provide high modularity and reliability, but the absence of the charging path and elongated discharging time intervals may lead to adverse drooping

of capacitor voltage. Thus, a large capacitor is required to limit the ripple voltage, also, the increase in the capacitor size results in sluggish output response and increases cost. Though the average currents are low in these topologies, the capacitor peak currents are high, resulting in high current rated switches. Thereby, derates the device utilisation and also increases the cost. This paper proposes a new boost DC-link integrated multilevel inverter (BDIMLI), which overcomes the limitations of existing SCMLI topologies. Besides, the proposed inverter provides 9-, 11- and 13-level operations with less component count, reduced capacitor size, adjustable voltage gain. The experimental results and comparative analysis of proposed BDIMLI are presented.

PHOTOVOLTAIC MODULE:

Modelling is the basis for computer simulation of a real system. It is usually based on a theoretical analysis of the various physical processes occurring in the system and of all factors influencing these processes.. The most common model used to predict energy production in photovoltaic cell modeling is the single diode circuit model that represents the electrical behavior of the pn- junction is given in fig 1 Figure shows how photovoltaic system works. The ideal photovoltaic module consists of a single diode.

A solar cell is the building block of a solar panel. A photovoltaic module is formed by connecting many solar cells in series and parallel. Considering only a single solar cell; it can be modeled by utilizing a current source, a diode and two resistors. This model is known as a single diode model of solar cell

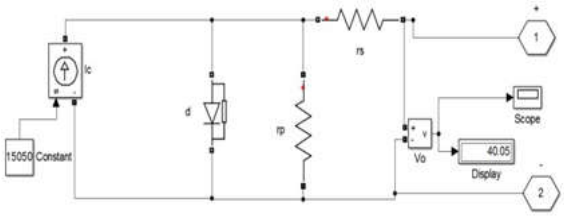


Figure : Single diode model of a solar cell

PHOTOVOLTAIC INVERTER

The PV power generation system consists of following major blocks:

1. PV unit
2. Inverter
3. Grid
4. MPPT

Analytical models are essential in the dynamic performance, robustness, and stability analysis of different control strategies. To investigate these features on a three-phase grid connected PV system, the mathematical model of the system needs to be derived. The modeling of the proposed system includes:

Photovoltaic Cell and PV array Modeling2.Three-phase inverter model

Three-phase fundamental transformations modeling

In this chapter, the operation and role of each of these components will be described and their mathematical model will be derived.

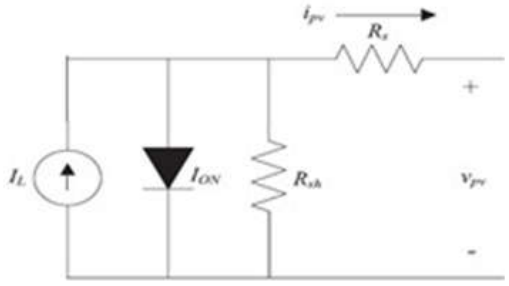


Fig. Equivalent circuit diagram of the PV cell **diode** D and capacitor C. Conv-2 is a level selector circuit comprising of two switches SL and SU, that makes the output voltage vo across the load

MPPT (Maximum Power Point Tracking)

The P&O algorithm requires few mathematical calculations which make the implementation of this algorithm fairly simple compared to other techniques. For this reason, P&O method is heavily used in renewable energy systems.

Perturb and Observe algorithm

At present, the most popular MPPT method in the PV systems is perturb and observe. In this method, a small perturbation is injected to the system and if the output power increases, a perturbation with the same direction will be injected to the system and if the output power decreases, the next injected perturbation will be in the opposite direction.

The Perturb and observe algorithm operates by periodically perturbing (i.e. incrementing or decrementing) the array terminal voltage and comparing the PV output power with that of the previous perturbation cycle.

If the PV array operating voltage changes and power increases, the control system moves the PV array operating point in that direction, otherwise the operating point is moved in the opposite direction.

In the next perturbation cycle, the algorithm continues in the same way. The logic of algorithm is shown in Fig.3. A common problem in perturb and observe algorithm is that the array terminal voltage is perturbed every MPPT cycle, therefore when the maximum power point is reached, the output power oscillates around the maximum power point resulting in power loss in the PV system.

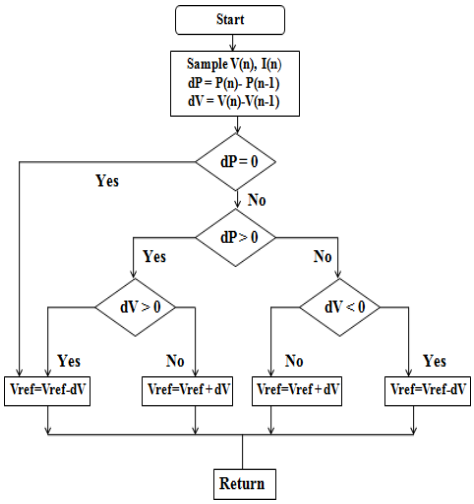


Fig. Flow chart of perturb and observe

PROPOSED DESIGN

Two-level boost DC-link converter (TBDC)

Fig. depicts the TBDC schematic, which comprises of two converters, namely conv-1 and conv-2. Conv-1 is a modified boost converter consisting of voltage source Vi , inductor L, boost switch Sb, resistance Ro equal to either Vi (level-1) or Vi + vc(level-2), where vc is the voltage across the capacitor C. Corresponding equivalent circuits of TBDC for level-1 and level-2 are shown in Figs. 2a and b, respectively. Fig. 2c illustrates the waveforms of TBDC, explaining its operation and control. Figs. 3a and b depict the typical output voltage waveform for conventional SCMLI basic cell and the TBDC unit, respectively. This clearly shows the drooping voltage during level-2 in the conventional SCMLI basic cell. The duration of level-2 decides the capacitor ripple voltage and its capacitance. Longer the duration, the larger will be the capacitor ripple or capacitance required. Operating modes of TBDC for level-1 and level-2 are explained as follows:

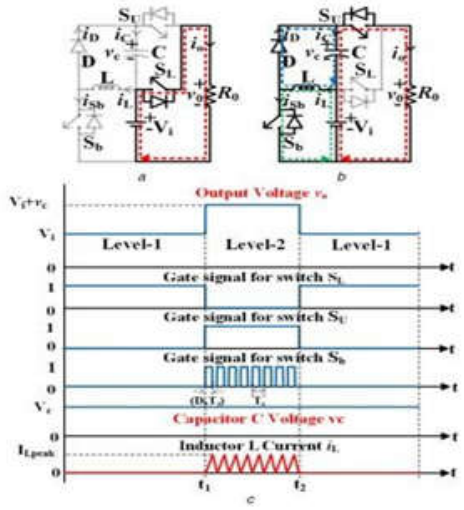

Output Voltage
Level-1
Level-2
Level-1
Gate signal for switch
Gate signal for switch
Gate signal for switch
Capacitor C Voltage vc
Inductor L Current
a
b
c

Fig. TBDC (a) Equivalent circuit for level-1, (b)Equivalent circuit for level-2, (c) Waveforms of the output voltage, switch gate pulses, capacitorvoltage and inductor current during level-1 andlevel-2 operations

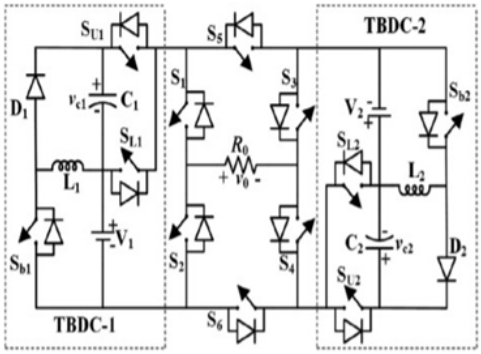


Fig. Schematic diagram of the proposed BDIMLI Design and operation of BDIMLI topology:

The schematic diagram of the proposed BDIMLI is depicted in Fig. 4. It consists of two TBDC converters and one hybrid H bridge formed by six switches (S1 − S6). The capacitors C1 and C2 are charged to the voltages Vc1 and Vc2, respectively, where Vc1 is n1 times of V1 and Vc2 is n2 times of V2. The TBDC-1 output voltages are V1 and V1 + Vc1 for the respective conduction of SL1 and SU1. Similarly, TBDC-2 output voltages are V2 and V2 + Vc2 for the respective conduction of SL2 and SU2. Fig. 5 depicts the logical realization of gate pulses for switches Sb1 and Sb2, which are synchronized with gate pulses of SU1 and SU2, respectively. Db1 and Db2 are the duty cycles of Sb1 and Sb2, respectively. The BDIMLI achieves 9 or 11 or 13-level output voltage waveform by proper selection of Vc1 and Vc2. Table 1 provides the respective capacitor voltages and step-up ratios (n1 and n2) for 9-, 11- and 13- level operations of BDIMLI. The switching states for 13-level operations are furnished in Table 2 respectively. The timing sequence and

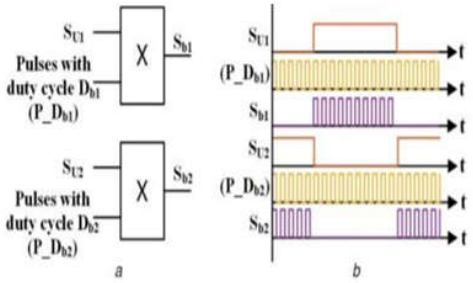


Fig. Sb1 and Sb2 gate pulses

(a) Logic diagram, (b) Model waveforms

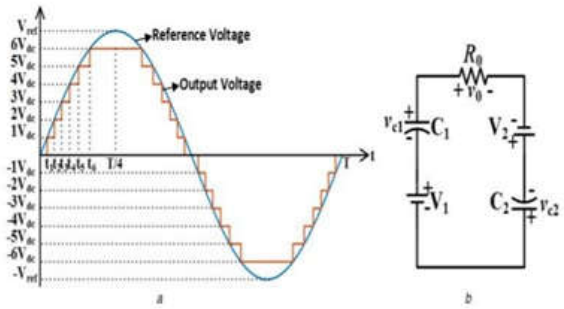


Fig. BDIMLI switching modulation logic anddesign

Corresponding switching states for each level ofthe 13-level output voltage are realized from Fig.6a and Table 2. Similarly, the timing sequence and switching states for each level of 9- and 11-level output voltages can be realized. Fig. 7 illustrates the equivalent circuits for each level of 13-level BDIMLI operation. The generalized output voltage of BDIMLI is given by

$$v_o = v_{o1}[(S_3 + S_4)(S_1S_6 - S_2S_5)] + v_{o2}[(S_1 + S_2)(S_3S_6 - S_4S_5)] \quad (11)$$

Where

$$v_{o1} = [S_{L1} + (1 + n_1)S_{U1}]V_1$$

$$v_{o2} = [S_{L2} + (1 + n_2)S_{U2}]V_2$$

4.1.1 For 9-level: From Table 3, it can be observed that the boost factor of BDIMLI is the same as existing 9-level SCMLI

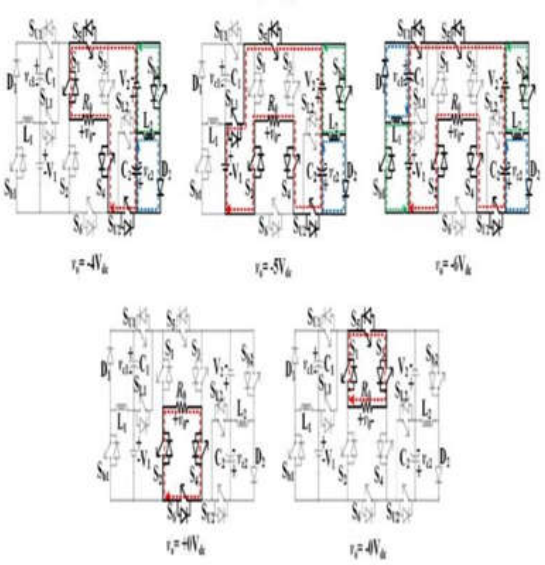


Fig.5.7 Different modes of operation of theproposed BDIMLI for 13-level operation

Topologies presented in [16, 18]. The size of the capacitors used for proposed BDIMLI is reduced by ∼60–100 times as compared with the other SCMLI counterparts. Topology presented in [9] requires less number of switches, but requires more number of sources and also lack of boosting capability. 4.1.2 For 13-level: From Table 4, it can be noticed that the proposed BDIMLI with high boost factor has reduced the count of switches as well as capacitors when compared with the other topologies presented. In this case, the capacitor size is reduced by ∼100 times in comparison with the other MLIs. Even though the proposed BDIMLI utilizes inductors, these are in terms of micro Henrys. Thus, it occupies less space and highly economical compared to the MLIs with bulky electrolytic capacitors. Further, the voltage and current stresses of the various switches presented inthe BDIMLI and the other step-up MLIs are provided in Table 5. The nearest rated components are considered for the cost comparison, which is also presented in Table 5. From this table, it can be observed that the cost of the capacitors used in the proposed topology is very less. Even though the BDIMLI utilizes additional components like voltage sensors and inductors, the overall cost is relatively lesser than the other step-up MLIspresented in Table 5.

SIMULATION RESULTS

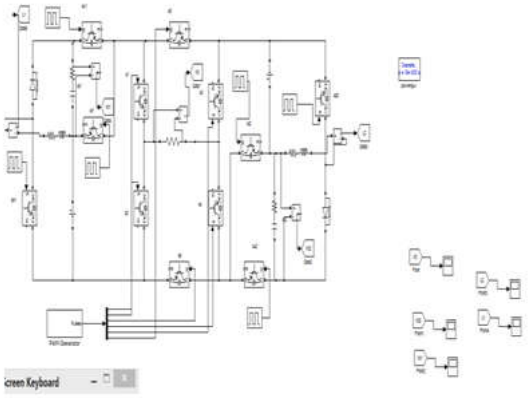


Fig. Simulink model of proposed system

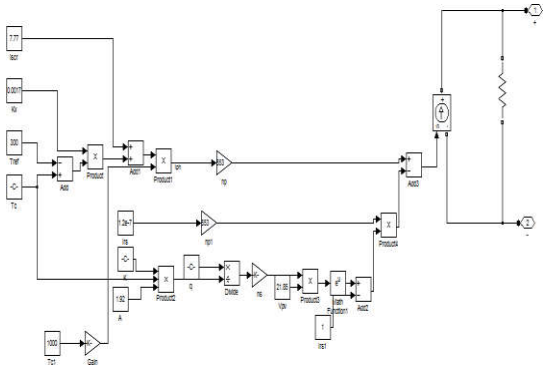


Fig .Simulink model of PV system

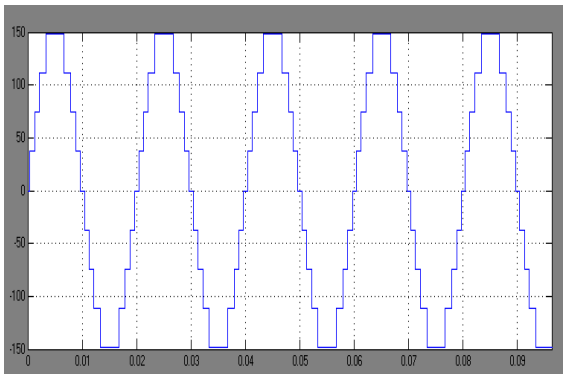
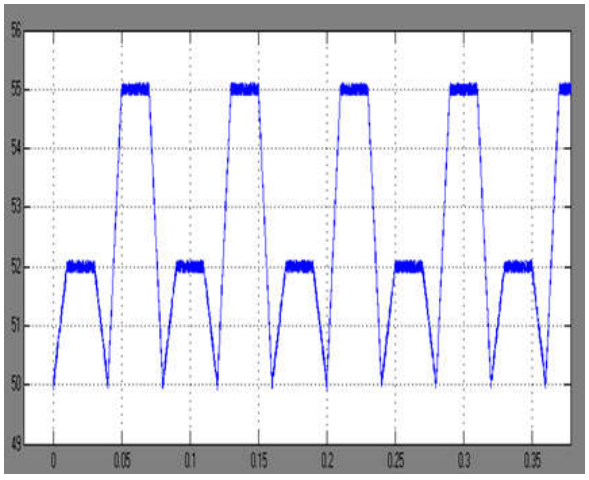


Fig. level output voltage



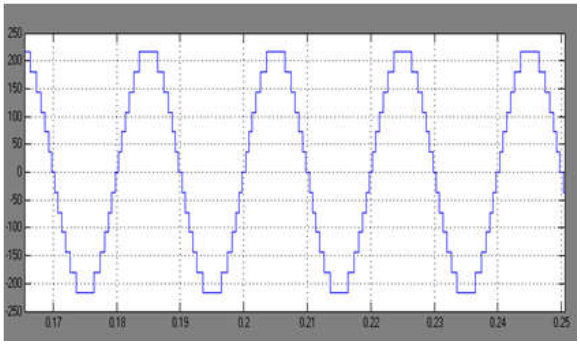


Fig 13 level output voltage

In this project, a novel boost DC-link integrated multilevel inverter connected to induction motor is proposed. The proposed BDIMLI provides various advantages such as high boost-factor, reduced capacitor size, relatively low cost, with low THD and component count. The design characteristics of inductors and capacitors are analyzed, which shows a significant reduction in capacitor size. In addition, the capacitor voltages are constant irrespective of load changing conditions for 9-level and 13-level operations. The benefits of proposed BDIMLI are justified with the comparative study in contrast to recent MLI topologies. Moreover, the dynamic behavior of BDIMLI under various load conditions is tested with

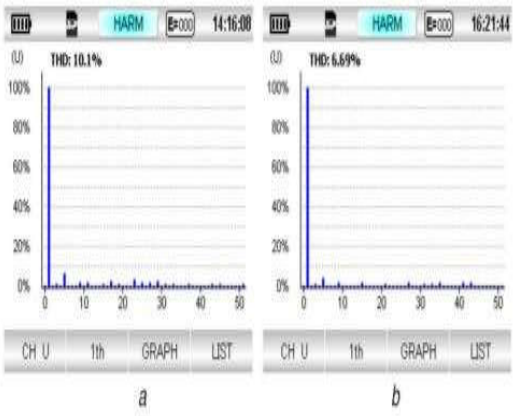


Fig. 7.1 Harmonic spectrum of load voltagev_o for

Fig 9 vc2 voltage 9-level operation, (b) 13-level **operation** No-load, resistive and inductive loads providing asmooth and stable operation

Conclusion:

Each area of electrical engineering, such as grid-tied renewable energy systems, electric cars, electric drives, etc., greatly expands the need of multilayer inverters (MLIs). MLIs offer superior output voltage compared to traditional two-level inverters, as well as decreased dv/dt, low switching frequency, smaller filters, and lower common-mode voltage (CMV) [1]. MLI topologies are often divided into three groups: cascaded H-bridge MLI (CHBMLI) [4, 5], flying capacitors MLI (FCMLI), and neutral-point clamped MLI (NPCMLI) [2, 3]. These MLIs are used by businesses linked to power quality and electric motors because of their impressive performance. NPCMLI and FCMLI topologies require a high component count (diodes, capacitors and its rectification circuitry to address voltage unbalance), while CHBMLIs need multiple isolated voltage sources. Thus, it leads to increased cost and reduced efficiency

REFERENCES

[1] Rodriguez, J., Lai, J.-S., Peng, F .Z. 'multilevel inverters: a survey of topologies, controls, and applications', IEEE Trans. Ind. Electron., 2002, 49,(4), pp. 724–738

[2] Rodriguez, J., Bernet, S., Steimer, P.K., et al.: 'A survey on neutral-point clamped inverters', IEEE Trans. Ind. Electron., 2010, 57, (7), pp. 2219–2230

[3] Pulikanti, S.R., Agelidis, V.G.: 'Hybrid flying- capacitor-based active-neutralpoint-clamped five- level converter operated with SHE-PWM', IEEE Trans. Ind. Electron., 2011, 58, (10), pp. 4643–465
[4] Hinago, Y., Koizumi, 'A single-phase multilevel inverter using switched series/parallel dc voltage sources', IEEE Trans. Ind. Electron., 2010, 57, (8), pp. 2643–2650
[5] Alexander, A., Thathan, M.: 'Modelling and analysis of modular multilevel converter for solar photovoltaic applications to improve power quality', IET Renew. PowerGener. 2015, 9, (1), pp.78–88
[6] Gupta, K.K., Ranjan, A., Bhatnagar, P., et al.: 'Multilevel inverter topologies with reduced devicecount: A review', IEEE Trans. Power Electron.,2016, 31, (1), pp. 135–151
[7] Sandeep, N., Yaragatti, U. R.: 'Design and implementation of active neutralpoint-clamped nine-level reduced device count inverter: an application to grid integrated renewable energy sources', IET Power Electron., 2018, 11, (1), pp. 82–91
[8] Su, G.-J.: 'Multilevel dc-link inverter', IEEE Trans. Ind. Appl., 2005, 41, (3), pp. 848–854
[9] Sonti, V., Dhara, S., Kukade, P., et al.: 'Analysis for the minimization of leakage and common mode currents in cascaded half-bridge PV fed multilevel inverter', IEEE J. Emerg. Sel. Top. Power Electron. 2019, 7, pp. 2443–2452
[10] Dewangan, N.K., Gupta, S., Gupta, K.K.: 'Approach to synthesis of fault tolerant reduced device count multilevel inverters (ftrdcmlis)', IET Power Electron., 2019, 12, (3), pp. 476–482
[11] Siddique, M.D., Mekhilef, S., Shah, N.M., et al.: 'Low switching frequency based asymmetrical multilevel inverter topology with reduced switch count', IEEE Access, 2019, 7, pp. 86 374–86 383