

## ANALYSIS ON USING BARREL SHIFTER TO DESIGN A HIGH SPEED, ACCURATE UNSIGNED MULTIPLIER

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### ABSTRACT

In error-tolerant applications, multiplication is essentially one of the key operations. As a result, the approximation multiplier method is considered effective in today's technology. The approximate multiplier will balance system performance and accuracy against energy consumption. In this study, a barrel shifter-based unsigned multiplier with excellent speed and accuracy is suggested. Here, the suggested system can choose the carry propagation value to meet the accuracy requirements. The partial product tree multiplier is used to estimate the proposed tree compressor. Utilizing a compressor and carry mask capable adder, the multiplier design is put into practice. In terms of energy, area, and latency, the suggested system performs better than the traditional multipliers.

**Key Words:** Unsigned multipliers, partial product generation, error analysis, area, delay.

### INTRODUCTION

Numerous widely used programmers, such as photo editing and recognition, are inalienably forgiving of minor errors. These applications are computationally demanding, and since they can handle an increase in users, there is a potential to trade off computational accuracy for lower power consumption. Fundamentally, a fault tolerant system results in undesirable behavior in applications. As a result, the trade-off between latency and power will produce precise results. The fault-tolerant application may be necessary in specific circumstances. This is mostly going to be utilized in the fault tolerance system programming phases. Here, the steps of the programmers will execute depending on the accuracy of the control. Precision is not needed if the accuracy is fixed. The precision is not set in the same manner that the precision is required.

Hence for diverse applications the precision requirement is necessary. There should be reconfigurable of multipliers in various program stages applications. So in this paper we designed a multiplier which will control the precision in effective way [1].

In this paper we used carry mask able adder and carry propagator adder are used. The carry mask able adder will organize the carries bit-parallel OR operations. In this configurability is used to control these carry mask able adder and carry propagator adder. In multiplier, the CMA is processed by using the tree structure. Because of this tree structure, there will be decrease in delay but there will be layer significant of tree. The main intent is to consume the power and increase the accuracy of the entire system. The partial product reduction will improve the speed of the system. The proposed multiplier consists of Brent Kung adder and parallel adder [2-3].

Enormous quantities of the DSP focuses execute picture and video taking care of figuring's where last yields are either pictures or chronicles organized human usages. This reality empowers us to utilize approximations for improving the speed/centrality ability. This begins from the constrained perceptual breaking points of people in watching a picture or a video. Notwithstanding the picture and video preparing applications, there are different zones where the precision of the math assignments isn't essential to the comfort of the framework. Being able to utilize the wrong getting ready outfits the creator with the farthest point of making tradeoffs between the exactness and the speed correspondingly as centrality use. Applying the estimation to the number juggling units can be performed at various courses of action reflection levels including circuit, technique for thinking, and design levels, likewise as tally and programming layers. The estimation might be performed utilizing

unquestionable approaches, for example, permitting some orchestrating infringement (e.g., voltage over scaling or over arranging) and point of confinement construe frameworks (e.g., changing the Boolean furthest reaches of a circuit) [4-5].

Adders and multipliers design the key parts in these applications. In unpleasant full adders are proposed at transistor level and they are utilized in cutting edge standard getting ready applications. Their proposed full adders are used as a touch of putting away of midway things in multipliers. To diminish gear multifaceted nature of multipliers, truncation is altogether used in settled width multiplier structures. By then a variable change term is added to make up for the quantization ruin displayed by the truncated standard. Frameworks in multipliers base on accumulating of midway things, which is fundamental as for control usage. Relaxed show multiplier is executed up, where the base fundamental bits of information sources are truncated, while binding halfway things to reduce gear multifaceted nature [6].

In most mixed media applications, individuals can accumulate valuable data from marginally wrong yields. In this way, we don't have to create precisely right numerical yields. Past inquire about in this setting abuses screw up quality essentially through voltage over scaling, utilizing algorithmic and compositional methodologies to direct the resulting botches. In this paper, we propose justification multifaceted design decline at the transistor level as an elective method to manage abuse the loosening up of numerical accuracy. We display this thought by proposing diverse free or vague full adder cells with lessened multifaceted nature at the transistor level, and use them to setup evaluated multi-bit adders. Despite the characteristic reduction in traded capacitance, our frameworks result in basically shorter fundamental ways, engaging voltage scaling. We structure designs for video and picture pressure calculations utilizing the proposed inexact number-crunching units and assess them to show the viability of our methodology [8].

## LITERATURE SURVEY

Approximate computing is an alluring worldview for advanced preparing at nanometric scales. Estimated processing is especially intriguing for PC math structures. The examination and structure of two new evaluated blowers for use in a multiplier. These plans depend upon various highlights of weight, to such an extent, that imprecision in calculation (as assessed by the foul up rate and the alleged standardized fumble clear) can meet concerning circuit-based figures of estimation of a structure. The fragmentary outcomes of the multiplier are changed to present moving likelihood terms. Reason whimsy of measure is moved for the aggregate of balanced divided things dependent on their likelihood.

The proposed guess is used in two assortments of multiplier. The need to support advanced sign handling (DSP) and course of action applications on imperativeness obliged devices has reliably created. Such applications routinely generally perform matrix increments using fixed-point number juggling while in the meantime appearing for some computational missteps. Accordingly, improving the imperativeness capability of duplication is essential. At long last, the exhibited computational mistake does not make any prominent effect on the nature of DSP and the precision of characterization applications.

The reconfigurable idea of FPGAs has settled on them an alluring decision for a wide scope of utilizations by lessening both an opportunity to promote, similarly as the related costs of developing new systems. In order to offer better than different applications, current FPGAs in like manner have hard DSP squares. These DSP squares are moved up to perform distinctive fixed point and floating point exercises, for instance, increase and division. Amalgamation devices will when all is said in done send these hard DSP squares to diminish the general execution time and power usages of different applications. So likewise, for a couple of uses, the utilization of DSP squares may result in exhaustion of the DSP impedes in at the same time running applications. Utilizing a FPGA-based precise  $n \times n$  multiplier setup, streamlined for district and essentialness capability, the novel duties of this paper consolidate an arrangement space examination technique for delivering assessed multipliers of emotional data sizes.

For each  $n \times n$  accurate multiplier, we give three derived  $n \times n$  multiplier designs by successful use of LUTs and pass on chains. In order to lessen the execution time of an  $n \times n$  multiplier, our system recommends realizing it using four events of  $n \times 2$  multipliers. Each individual case of  $n \times 2$  multiplier can be created either clearly or recursively from four events of  $n \times 4$  multipliers. Other than supporting accurate summation of midway things, we in like manner give a novel  $n$ -bit evaluated adder to decrease the general execution time of the multiplier. The sum total of what usage has been described by their territory and dormancy necessities and normal relative mistakes.

The hole between capacities of CMOS innovation scaling and prerequisites of future application outstanding tasks at hand is expanding quickly. There are a few promising plan approaches that together can diminish this hole fundamentally. Rough registering is one of them and as of late, has pulled in the most grounded consideration of established researchers. Rough figuring adventures inalienable mistake strength of uses and highlights superior vitality effective programming and equipment executions by exchanging off computational quality (e.g., exactness) for computational endeavors (e.g., execution and vitality). Throughout the decade, a few research endeavors have investigated inexact processing all through every one of the layers of figuring stack, be that as it may, a large portion of the work at equipment dimension of reflection has been proposed on adders. In, a similar overview of best in class estimated adders is given. Furthermore, it likewise gives correlation dependent on both customary structure measurements just as inexact processing plan measurements.

**EXISTED SYSTEM**

The below figure (1) shows the architecture of existed system. Basically, there are columns and rows in  $n$  bit multiplier. This  $n$  bit multiplier consists of partial product. This partial product reduction performs the operation in three stages. At last the carry propagator adder operation is performed in fourth stage. As shown in below figure (1) the dots are represented as the partial products. Depend on that dots the entire operation is performed. Coming to least significant digit the bit value is equal to zero and in the same way the most significant bit value is equal to 14. Here the right side of the diagram is denoted as most significant digit and in the same way the left side of the diagram shows as least significant digit. Coming to the blocks, the first square block in stage-1 is represented as ATC and the dashed lines in the square block are indicated as the iCACs. Here for every line the partial product will be there to perform the operation. After the entire operation is performed in the existed multiplier we can observe some indications. The partial product at the line  $o$  is represented as the main line in the system. Now let us discuss the each stage of operation in detail manner.

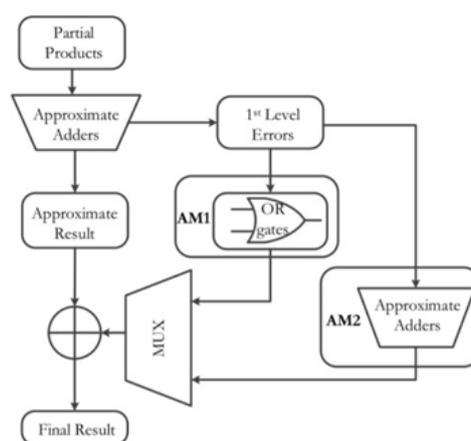


Fig. 1: EXISTED SYSTEM

Coming to stage 1, the partial products are divided into four segments  $p_1, p_2, p_3, p_4$ . Along with that the multiplier uses a vector  $v_1$  from ATC. Now when the operation starts, the four values of  $p_1, p_2, p_3$  and  $p_4$  will be diminished and follow the  $p_5$  and  $p_6$  segments. To diminish the two values we use the vector segment  $v_2$ .

Hence the stage 1 of existed system takes seven partial products to obtain the pack of four lines they are  $p_7$ ,  $v_1$ ,  $v_2$  and  $q_7$ . This is about the overview of stage 1, let us discuss about the operation of stage 2.

Here in stage 2 we utilize the bit values from 4 to 10 for further proceedings. The both vectors  $v_1$  and  $v_2$  use the OR gate for addition operation. Now these vectors  $v_1$  and  $v_2$  will find those address bits which are unfilled in the entire system. Hence to continue this operation we utilize the stage

3. Now half adders and full adders are used to address the bits in stage 3. Now first we allot the full adders and half adder's requirement to the system. The bits 1 and 13 use the two half adders and in the same way the bits 2 and 12 use the eleven full adders. Because of this there will be speed in operation. This is about the detail view of stage 3, now let us discuss about the stage 4.

Carry mask able adder and carry propagator adders are used in stage 4. The carry propagator adder will divide into four fragments for further processing's. Similarly, the carry mask able adder divides 6 fragments in the system. Hence the bits 0 to 4 will perform the OR operation to get the carries from precision bits. So the length of CPOA is varied. The length of the CPA in existed multiplier design is 13.

Since the upper bits are the most basic for precision, bits 12 to 14 are depicted as the exact part, and three cautious adders are utilized to make the qualities for these bits of the last outcome. The exactness controllable part lies between the truncated and cautious parts. This part is immense for both basic way deferral and accuracy. For each piece of S that is made by a 2- information OR section, control use is decreased in light of the manner in which that the exchanging advancement is reduced in a piece of the strategy for thinking gateways.

### PROPOSED SYSTEM

The below figure (2) shows the block diagram of proposed system. In this system we use partial product multiplier generator, accurate adder. The multiplication process is implemented in three stages, they are partial product generation, and partial product reduction tree and the vector merge addition. At last from this output is obtained from sum and carry generation through tree architecture. Here the approximation value is set to one by handling the approximation between actual output and approximate output. Hence the Carry outputs are approximated when Sum is approximated

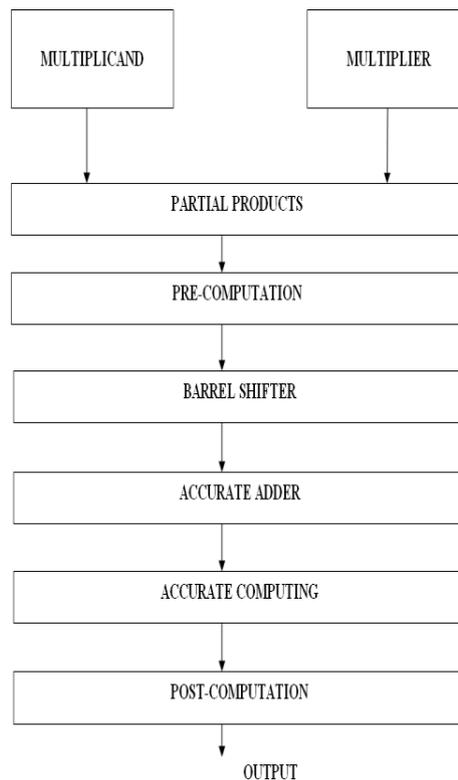


Fig. 2: PROPOSED SYSTEM

Here first data sources are taken from the tree design and arranging the board and given to partial product multiplier generator. This multiplier generator will duplicate the qualities and produce specific flag. Presently this proliferates and produce signals is trailed by razor flip flop. Razor flip will set the incentive to one to the framework to tell the mistake. After this we will ascertain postponement and zone. Presently given us a chance to examine about incomplete item generator and razor flip failure in detail way.

Digital multipliers are widely utilized in number approximate units of microchips, mixed media and advanced flag processors. Essentially, paired portrayal is utilized while planning multipliers. Numerous calculations and structures have been assigned to plan rapid and low power multipliers. A basic parallel product generation by advanced circuits contains three stages. In the initial step, partial items are delivered; in the second step, every incomplete item are included by a fractional item decrease tree still two incomplete item pushes be left finished. In the third step, the two partial product item pushes are summed up by a quick convey spread snake. Two strategies have been utilized to do the second step for the fractional item decrease. An item framed by increasing the multiplicand by one digit of the multiplier when the multiplier has more than one digit. Partial product is utilized as middle of the steps in figuring bigger items.

An accurate adder is a computerized circuit that performs expansion of numbers. The hybrid adder includes two double digits called as augends and numbers to be added and deliver two yields as aggregate and convey; XOR is connected to the two contributions to create total AND gate is connected to the two contributions to create convey. In numerous PCs and different sorts of processors adders are utilized in the number representation logic units or ALU.

They are additionally utilized in different pieces of the processor, where they are utilized to compute addresses, table files, augmentation and decrement administrators, and comparable tasks. In spite of the fact that adders can be developed for some number portrayals, for example, paired coded decimal or overabundance 3, the most well-known adders work on twofold numbers. In situations where two's supplement or ones' supplement is being utilized to speak to negative numbers, it is paltry to change a viper into an adder-subtractor. Other marked number portrayals require more rationale around the essential adder.

RESULTS

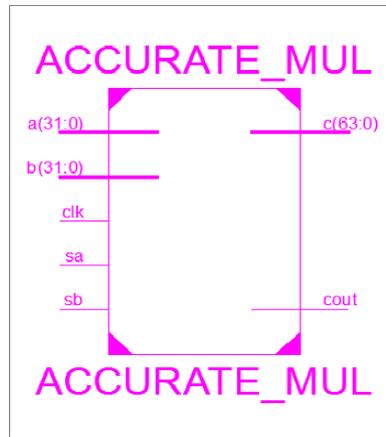


Fig. 3: RTL SCHEMTAIC



Fig. 4: TECHNOLOGY SCHEMTAIC

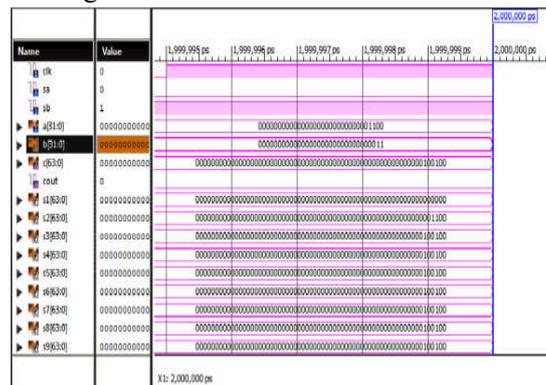


Fig. 5: OUTPUT WAVEFORM

CONCLUSION

In this study, barrel shifter-based unsigned multiplier architecture with great performance is proposed. With regard to area, latency, and accuracy, this unsigned multiplier produces good results. Product perforation is assessed using a wide range of multipliers to reduce system mistakes. However, the suggested system achieves high quality metrics operation despite the usage of several approximation strategies. Applications for image processing mostly use this. Finally, an application-level assessment proved that our suggested multiplier could

manage accuracy.

## REFERENCES

- [1] Tongxin Yang, Tomoaki Ukezon, Toshinori Sato, "A Low-Power High-Speed Accuracy-Controllable ApproximateMultiplier Design" 978-1-5090-0602- 1/18/\$31.00 ©2018 IEEE.
- [2] S. Hashemi, R. I. Bahar, and S. Reda, "DRUM: A Dynamic Range Unbiased Multiplier for approximate applications," IEEE/ACM International Conference on Computer-Aided Design (ICCAD), pp. 418- 425, Nov. 2016.
- [3] B. Moons, M. Verhelst, "DVAS: Dynamic Voltage Accuracy Scaling for increased energy-efficiency in approximate computing," IEEE/ACM International Symposium on Low Power Electronics and Design (ISLPED), Jul. 2015.
- [4] A. Momeni, J. Han, P. Montuschi, and F.Lombardi, "Design and analysis of approximate compressors formultiplication," IEEE Transactions on Computers, vol. 64, no. 4, pp. 984-994, Apr.2015.
- [5] Z. Yang, J. Han, and F. Lombardi, "Approximate compressors for ErrorResilient multiplier design," IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFTS), pp. 183- 186, Oct. 2015.
- [6] R. Anithal (Prof.), Sarat Kumar Sahoo (Prof.),"A 32 BIT MAC Unit Design Using Vedic Multiplier and Reversible Logic Gate" in International Conference on Circuit, Power and Computing Technologies [ICCPCT] 2015.
- [7] C. Liu, J. Han, and F. Lombardi, "A Low-Power, High-Performance approximate multiplier with configurable partial error recovery," Design, Automation & Test in Europe Conference & Exhibition (DATE), Mar. 2014.
- [8] S. Venkataramani, V. K. Chippa, S. T. Chakradhar, K. Roy, and A. Raghunathan. "Quality programmable vector processors for approximate computing," 46th Annual IEEE/ACM International Symposium on Microarchitecture (MICRO), pp. 1-12, Dec. 2013.
- [9] G.Ganesh Kumar, V.Charishma, "Design of High Speed Vedic Multiplier using Vedic Mathematics Techniques", International Journal of Scientific and Research Publications, Volume 2, Issue 3, March 2012 .
- [10] H. R. Mahdiani, A. Ahmadi, S. M. Fakhraie, and C. Lucas, "Bio-Inspired imprecise computational blocks for efficient VLSI implementation of Soft-Computing applications," IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 57, no. 4, pp. 850-862, Apr. 2010.
- [11] Fatemeh Kashfi, S. Mehdi Fakhraie, Saeed Safari," Designing an ultra-high- speed multiply-accumulate structure", Microelectronics Journal 39 (2008) 1476–1484.
- [12] K. J. Raghunath, et al. "A compact carry-save multiplier architecture and its applications," Proc. IEEE 40th Midwest Symp. Circuits and Systems, vol. 2, pp. 794-797, Aug. 1997.