DESIGN OF ALU BY REDUCTION OF DELAY AND ENERGY CONSUMPTION USING QUANTUM DOT CELLULAR AUTOMATA

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ABSTRACT

The Arithmetic Logic Unit (ALU) is a fundamental component of the Central Processing Unit (CPU)which carry out arithmetic and logical operations. To design an ALU using Quantum-Dot Cellular Automata, which is a novel promising nano-scale technology that allows the design of integrated circuits. QCA can be considered as the most appropriate alternative for CMOS technology in terms of area, cell count, power consumption and delay. In present VLSI Technology power consumption and delay has become a very important fact for consideration. By using Reversible gates for designing ALU with reduced power consumption and delay while compared to the conventional design-based circuits. The concept of reversible logic design permits fully invertible computation. In this paper design of ALU with reduced energy consumption and delayare presented. The proposed structures discuss the use of Double Peres Gate, n×n Feynman gates, The proposal uses n×n Feynman gates and Double Peres Gate. The proposed design also reduces the garbage values. The proposed designs have better performance in terms of area, energy consumption and delay. QCAD and QCAD-Pro are used to simulate the proposed design.

INTRODUCTION

CMOS technology is by far the most popular method for producing integrated circuits. CMOS stands for complementary metal oxide semiconductor. Many electrical components, including microprocessors, batteries, and digital sensors, utilise this technology. A large number of logic processes are also possible with CMOS on a single chip.This is primarily the reason that CMOS became the technology that was employed in VLSI chips the most. The technology utilised in CMOS transistors is called a MOSFET (metal-oxide semiconductor field-effect transistor). As a result, CMOS circuits have the advantages of a simple design, low power consumption, good noise tolerance, and strong temperature stability, which facilitates high integration. Due to the great level of integration, the entire circuit is also integrated onto the chip.

Extensive research and testing allowed the creation of nanotechnology as well as a practical substitute for complementary metal-oxide semiconductor (CMOS) technology. In order to strengthen the foundations of QCA technology and the way that logic circuits are built, the essay gives a thorough analysis. the comparison and discussion of several QCA-based circuits now in use for various parameters. The Quantum-dot Cellular Automata (QCA), a nano-scale computer fabric, is being studied by the VLSI research group as the difficulties involved with downsizing CMOS transistors become more severe.

Digital information is encoded using electron polarization. It is more appealing than CMOS technology because of its larger size, quicker speed, feature, high degree of scalability, greater

switching frequency, and low power consumption. Quantum-dot cellular automata (QCA), a new technology, circumvents the physical limitations of the MOS chip. QCA is a dynamic computational transistor paradigm that addresses concerns with device density, power, operating frequency, and connections.

Quantum dot cellular automata (QDCA, also known as quantum cellular automata or QCA), have been developed as an enhancement to traditional computer architecture, in accordance with John von Neumann's classical models of cellular automata (CMOS). The Quantum-dot Cellular Automata (QCA), a nano-scale computer fabric, is being studied by the VLSI research group as the difficulties involved with downsizing CMOS transistors become more severe. The power needs of the MOS device can be reduced by device scaling. Quantum dots, which are nanostructures, are made from common semi-conductive materials.Three-dimensional (3D) quantum energy wells can be used to simulate these structures. Logical operations and data transport are performed via the Columbic contact between neighbouring QCA cells rather than the current flow. Quantum-dot cellular automata (QCA), a new technology, circumvents the physical limitations of the MOS chip. QCA is a dynamic computational transistor paradigm that addresses concerns with device density, power, operating frequency, and connections.

Introduction to QCA

A type of nanotechnology known as transistor less technology is quantum dot cellular automata. The majority gates of AND, OR, and NOT make up the QCA's fundamental building blocks. This advanced technology does not allow the flow of electrons for information transfer rather it allows polarization of charge. Due to the special characteristics that emerge at such small feature sizes, nanotechnology opens up new possibilities for computing. Quantum-dot Cellular Automata is one of these novel devices that depends on novel physical phenomena like columbic interactions and cutting-edge methodologies that diverge from a CMOS-based paradigm. In order to efficiently build large-scale QCA systems, new design approaches are required because the QCA system uses fundamentally distinct processing paradigms. In addition, QCA technology may be used to get around CMOS technology's restrictions.

A very symmetric QCA cell structure, extremely high switching rates, extremely high device densities, functioning at room temperature, and even the potential for self-assembly of devices in large quantities are all projected benefits of such a technique.

The majority of CMOS technology's shortcomings are mostly resolved by QCA, but it also has drawbacks of its own. According to research, a QCA cell's intrinsic switching time is, at most, in the order of terahertz. However, due to the correct quasi-adiabatic clock switching frequency configuration, the real speed may be significantly lower, in the range of gigahertz for molecular QCA and megahertz for solid state QCA.

LITERATURE SURVEY

An area-efficient coplanar, reversible arithmetic and logic unit based on quantum-dot cellular automata technology was presented by Rama Krishna Reddy Venna et al., and G. Durga Jayakumar *et al.,*[1] employing double Peres and Feynman gates. The suggested arithmetic and logic unit executes 19 arithmetic and logic operations with a delay of 2.5 clocks and a total size of 0.1 μm^2. Moreover, the average energy dissipation is 4.95e003 *eV*, while the total energy dissipation, as determined by QCA Designer-E, is 5.45e002 *eV*.

The output signal strength of the efficient fault-tolerant three-input majority gate presented by

Ahmadpour, and RasouliHeikalabad, Saeed *et al*., [2] is extremely high 9.93e-001, and it has ten simple and rotating cells. The suggested structure's fault tolerance is examined for cell omission, extra-cell deposition, and displacement flaws. Ultimately, a fault-tolerant one-bit arithmetic logic unit with four logical and mathematical operations is developed and constructed utilising the suggested circuits.

An enhanced single-bit arithmetic logic unit for quantum dot cellular automata was proposed by Saeed RasouliHeikalabad et al., and MahyaRahimpourGadim*et al*., [7]. The suggested structure for an ALU includes the operations AND, OR, XOR, and ADD. The suggested structure makes use of a special 2:1 multiplexer, a super-efficient two-input XOR, and a complete adder with low complexity. This ALU employs coplanar cross wiring, has a 0.29 m^2 occupied area, 257 cells, and a 2-clock cycle delay. Cross wiring of 90-degree cells with several clock zones is employed in this design.

Reversible fault-tolerant logic synthesis for the Field Programmable Gate Array (FPGA) and its realisation using MOS transistors are proposed by Md. Shamsujjoha et al., Hafiz Md. Hasan Babu et al., and Lafifa Jamal *et al*., [10]; introduced a small reversible fault tolerant was created utilising an FPGA's Plessey logic block, n-to-2n decoder, 4n-to-n multiplexers, random access memory, and other components.

PROPOSED ALU DESIGN

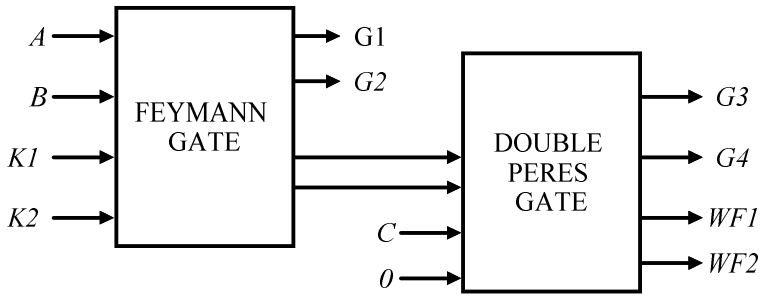


Fig.1 Proposed ALU Design

The Figure.1 demonstrates the proposed ALU. The proposed ALU has 6 inputs and 6 outputs in which 4 four outputs are garbage values which are useless.The inputs K1 and K2 are the control signals used to select the required arithmetic or Logic function [11]. While performing the logic functions, the input 'C' is also treated as a control signal. G1, G2, G3, and G4 are all unusable outputs. The QC of the DPG gate is six and each Feynman gate is one. So, the total proposed ALU's QC is calculated as eight. The XOR and XNOR functions are performed on the output WF1, while the other logic functions are generated on the output WF2. To conduct arithmetic operations, the outputs WF1, and WF2 are combined.

The garbage outputs G1 and G2 are producing the inputs 'A' and 'B' are useful in the next step of operations whenever the same input has to be applied to different reversible logic gates. The garbage output G3 is used to produce the complemented output of the input 'A' based on the control input K1. The garbage output G4 is useful to generate the XOR and XNOR functions between the operands 'A' and 'B' based on the applied control inputs K1 and K2.

$G1 = A;$ (1)

$G2 = B;$ (2)

$G3 = A \oplus K1$ (3)

$G4 = (A \oplus K1) \oplus (B \oplus K2)(4)$

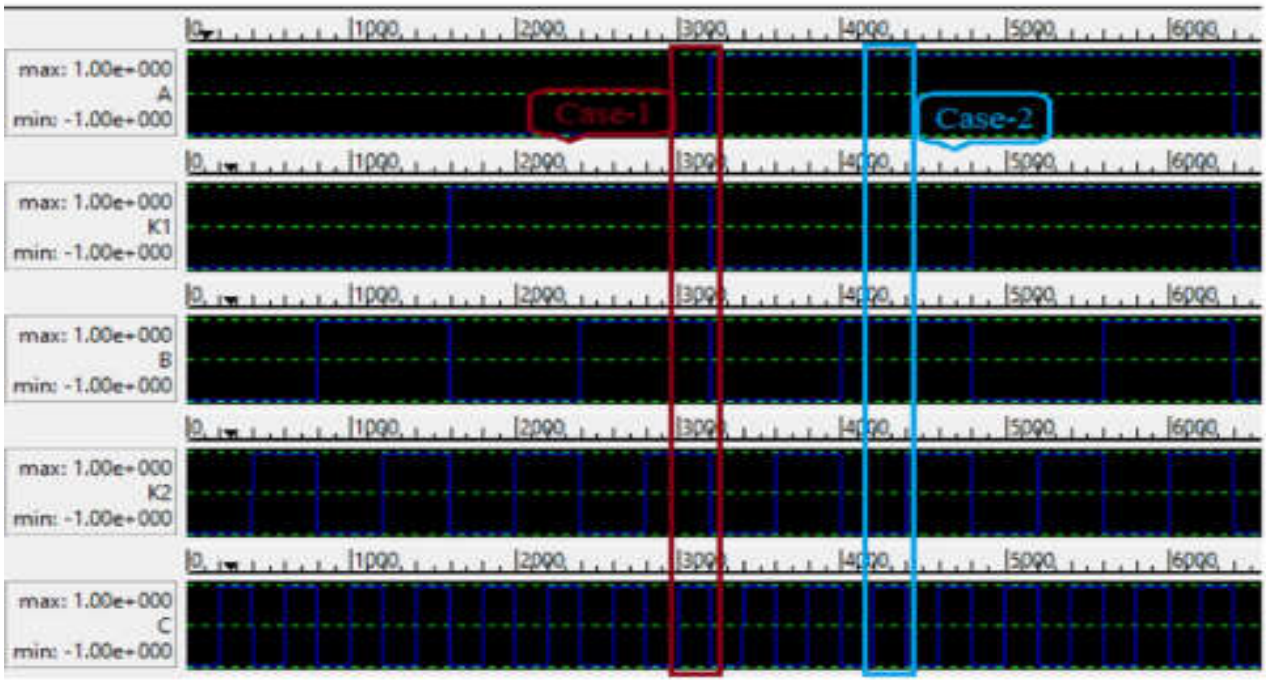
$WF1 = (A \oplus K1) \oplus (B \oplus K2) \oplus C\ (5)$

$WF2 = (A \oplus K1) \oplus (B \oplus K2)C \oplus ((A \oplus K1)(B \oplus K2))\ (6)$

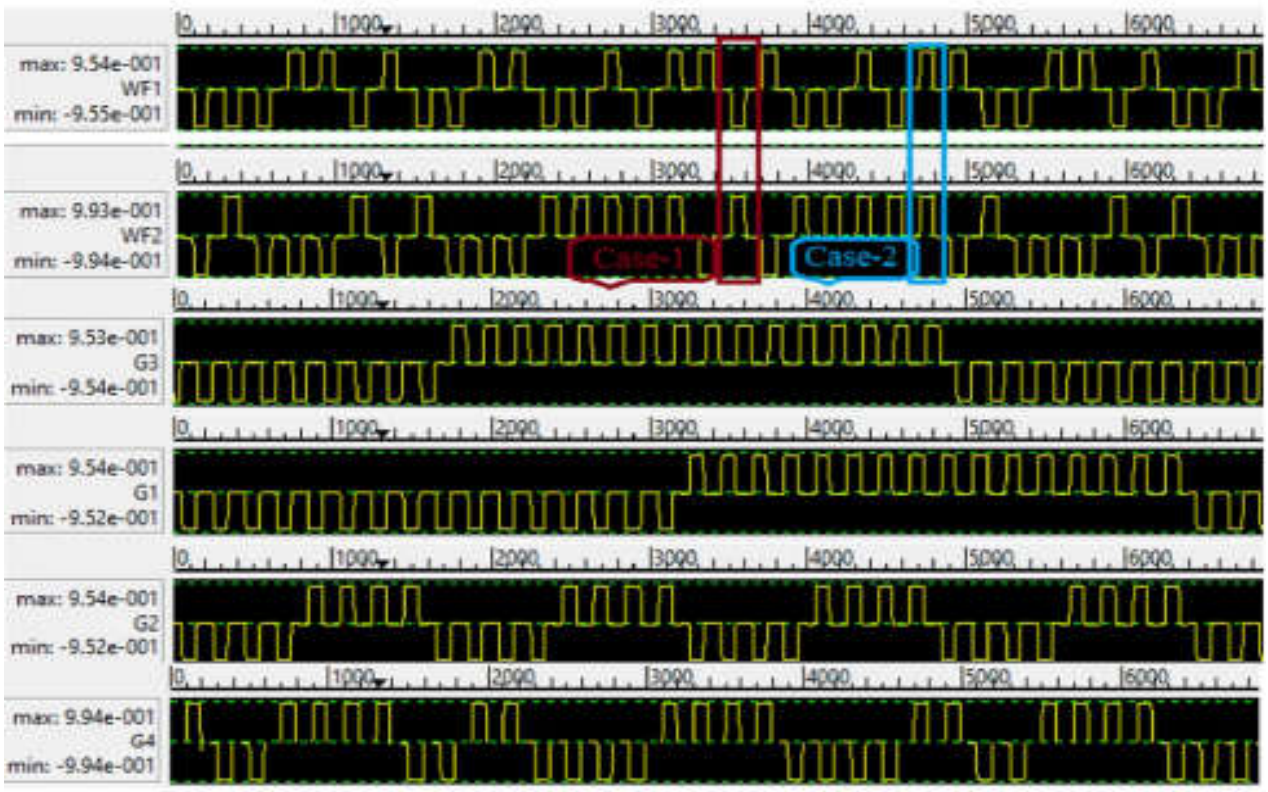
This ALU is implemented in a single-layer architecture, i.e., coplanar design model and no wire crossings are used in this QCA cell structure. In this case of garbage, output latency is not considered. The proposed ALU can perform the logic operations, namely XOR, XNOR, AND, OR, NOR, and NAND, and arithmetic operations namely clear, set, reset increment, and addition.

RESULTS AND DISCUSSIONS

Using the default parameters of the QCAD esigner, the suggested ALU is simulated in bistable simulation with a cell size of 1818 nm2, a quantum dot diameter of 5 nm, a sample size of 12800, and a convergence tolerance of.0.001, the effect radius is 65 nm, clock high is 9.8e 022J, relative permittivity is 12.9, clock low is 3.8e 023J, clock amplitude factor is 2, layer spacing is 11.5 nm, and maximum sample iterations are 100. Once the circuit layout is finished, variables for the associated design, such as cell occupied area, number of cells, and delay, can be extracted.



(a)



(b00)

Fig.2 Simulation results of proposed ALU a input waveforms, b output waveforms

CONCLUSION

In this work, the proposed ALU design is compared with previously published studies to demonstrate that it outperforms those ALUs. The results collected support the QCA design's capacity to dissipate less energy. This is a significant discovery because it supports the use of QCA research to overcome the physical constraints imposed by traditional computing methods. The results of the investigation have greatly accelerated this course.

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