CREATING A PARALLEL PREFIX ADDER ERROR DETECTION AND CORRECTION SYSTEM THAT IS HIGHLY EFFECTIVE

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ABSTRACT

Due to the intricacy of the circuit, there is significant power consumption during VLSI circuit design. It is common knowledge that the need for portable equipment is rising quickly right now. In many arithmetic logical functions, adders are a crucial component. The circuit for binary addition that has been created is called the Parallel p Prefix Adder. The ability to fabricate a VLSI chip using their unique configuration and execution performance is quite great. The design and functionality of the adjustable Parallel h Adders for approximation computing, built by utilizing multiple design methodologies, are proposed in this study. Delay, gate count/transistor count (area), and power calculations are used to estimate the performance of a parallel adder. Here in this proposed system analyzing the performance of parallel adder by computing test parameters several times and compared against conventional adder.

Key Words: Parallel adders, approximate computing, Configurable adder

I.INTRODUCTION

The four fundamental operations of addition, multiplication, division, addition, and subtraction are the most important ones. Addition is a crucial operation in every digital system [4]. All subsequent arithmetic operations may be carried out using this fundamental action. The device speed is immediately increased by [2], which is used to create a quick, accurate, and low power adder. This adder may be used to speed up computations and extend the overall life of the system. Digital systems including Digital Signal Processors (DSP), microprocessors, microcontrollers, and other data processing units are built around the Arithmetic and Logic unit [6]. An adder is a crucial component of many arithmetic operations as a hardware unit for all other applications.

The addition function is also used in various other functions like decoding, encoding and so on. Generally, addition is a function of adding two numbers which produces the output known as the sum and the carry. All the complex adder structures are developed using Half Adder (HA) and Full Adder (FA)only.

The complete basic function of adder is constructed using a Half Adder and this can be improved by a Full Adder. The carry bit which is obtained in the addition process is very important in the design of an adder and also decides the speed of the adder. To reduce the time delay of the propagated Carry, multiple adders are designed. Binary adder is one of the significant modules of microprocessors. It is not only used to complete addition and subtract functions, but also can be used to achieve multiplication functions and so on. Some of the mostly used adders are CLA [1], Manchester Chain Adder, Carry Select Adder and Parallel Prefix Adder.

Designing of an adder consist a lot of constraints. The trade-off between the delay and the area is the important factor. Usually adder requires very less area that's why it is easy to implement, but the time taken to givethe result is high. To overcome this, advanced techniques are coming in to picture. Now a day's including the speed, the power consumption is also aconsiderable parameter. So the design of an adder is useful to satisfy all the specifications [5].

Binary addition is the basic function that continuously plays a considerable effect on the modern-day digital system design like control systems and DSP circuits. Various types of adders are available in which each one

has its own importance and performance. Selection of an adder is based on the specific use of that. Therefore, binary adders are needed to have fast computation time, high efficiency, less area and low power consumption.
Binary adder [3] is the most important element in any digital system and determines the performance of that digital system. It is used in many applications like arithmetic and logic units, multipliers, memory addressing units and dividers. Implementation of binary adder with advanced technology improves the overallperformance of the device as well as entire system. The main disadvantage of this adderis the carry chain. The number of input bits available at the input of the adder increases the length of the carry chain. To increase theefficiency of the carry propagate adder, it is need to extent the carry chain without eliminating it. So, most of the digital designers now a day's came with high speed adder by advancing the architecture of computer which tends to keep the criticalpath in many calculations. In this paper mostly concentrated on the designing of an adder with high speed, device utilization andusage of cell.

RELATED WORK

In electronics adder performance addition operations. Adder exits in ALU, some Arithmetic logic units contain multiple adders. Adder can construct based on numerical expressions, such as Excess-3 or binary coded decimal (BCD), most of the adders operates on binary numbers. For single bit addition, two types of adders are there. Consider A and B are two inputs of half adder and outputs are sum S and Carry Co. S is the XOR operation of two inputs A and B, and Co is the AND operation of two inputs A and B. perhaps output of Half adderis sum of two bit numbers, and Co be the most significant number. Second type of adder is full adder; it contains three inputsA, B and Ci. A full adder is constructedbased on two half-adders.
Multi-bit adders are several types in that ripple carry adder are simple, as well as slowest, since it propagate each full adder. Carry look ahead adder is work by creating and propagate from a few significant bit position. In some cases P is nothing but sum of the output of a half adder and G is carry output for generation adder. P and G create carries of bit position. Multi bit architecture breaks the adder into blocks. To reduce time blocks required the carry length of circuits, this block based on carry bypass adder. Hereeach bit is determined by p and g values from each block.

Half adder:

A and B are two single bit numbers , Half adder is used to add these two numbers and produces sum 'S' and Carry out Co. Half adder uses only two single digit numbers.For lager adding circuits like Full adders it may be used as stating building block. Boolean expressions are

$S = A \oplus B = A^1B + AB^1$ (1)

$Co = AB$ (2)

Full adder:

Consider A, B and C are three inputs of Full adder and outputs are Sum 'S' and Carry'Co'. Full adder is constructed in series connection by using two half adder. The sum of A and B are fed to the second half- adder, which then adds it to the carry in C to generate final output S. the Carry out , Co, isthe result of an OR operation obtained.

Parallel adder

Parallel adders carry outputs of both halfadders. are constructed with basic digital circuits which computes the addition operation of binary equivalent in parallel manner.
Basically, Ripple carry adder is a circuit which produces arithmetic sum of twobinary numbers. The RCA is composed of a cascade of full adder blocks. Although the RCA is composed of a simple structure, which enables easy implementation and presents poor performance, because of the carry is propagated into each

addition block.In this, each carry bit is rippled into the next stage. But here delay is obtained in the circuit. The delay of reverse converters will bind the growth of logarithm in Parallel prefix adder. Basically, in RCA large number of adders will be used. The bit length of this adder is very large.

To perform the first part of addition in the system, desired structures with particular operands are used. High power consumption is obtained due to the recursive effect. Recursive effect is obtained while generating and propagating the signals at prefix level. High fan out characteristic also obtained in the system. So to overcome the problem of delay occurred in the system, a new system is proposed. However, this problem is eliminated by using additional prefix level which is discussed in below section. In contrast to the proposed system, it is able to perform a conditional increment depending upon the control signals.

EXISTED SYSTEM

The below figure (1) shows the architecture of existed system. The existed system designed with accuracy-configurable adder by masking the carry propagation at runtime. This adder accomplishes the actual function of delivering an unbiased trade-off amid power and delay with no loss of reliability. In general, a CLA has of three parts:

(1) Half adders for carry production (G) and propagation (P) signals preparation,

(2) Carry look-ahead units for carry generation, and

(3) XOR gates for producing final sum.

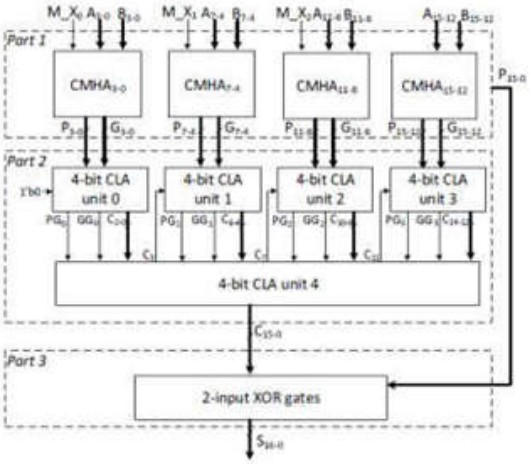

Fig. 1: EXISTED SYSTEM

Here, half adders for G and P signals ground work in part 1 Note that owing to exploit the circuit of A_i XOR B_i for S_i production, here P_i is indicated as A_i XOR B_i in its place of A_i OR B_i. As C_0 is same as G_0, if G_0 is 0, C_0 will be 0. From figure (2), C_1 is equal to G_1 when C_0 is 0. In otherwords, if G_0 and G_1 are equal to 0, C_0 and C_1 will be 0. By expanding the above to i, C_i will be 0 when G_0, G_1, … , G_i are all 0. This means that the carry propagation from C_0 to C_i is masked. From (3.1 hen $M\_X_i = 1$, the exact sum S_i and carry C_i will be 0 and 1 ($\{C_i , S_i\} = \{1,0\}$); when M_X_0 , M_X_1 , …

, M_X_i are all 0, S_i is equal to P_i (= A_i XOR B_i = 0) as an approximate sum and C_i is equivalent to 0 ($\{C_i , S_i\} = \{0, 0\}$) as conferred above. Here {,} denotes concatenation.

This denotes that the variation amid the exact and estimated sum is 2. Headed for improved reliability results for the estimated sum, by using an OR operation as an alternative to an XOR operation for P production when M_X = 0. Hence, the disparity will be decreased to 1. A 2-input XOR gate can be developed by using a 2-input NAND gate, a 2-inputoOR gate, and a 2-inputtAND gate.), obtain that S_i is similar to P_i when C_{i-1} is 0. From the standpoint of near computing, if G is controllable and can be controlled to be 0, the carry propagation will be masked and S (=P) can be taken as a fairly accurate sum. The other way of perception, get hold of the selectivity of S amid the accurate and approximate sum if G is to be A AND B or 0. But this system doesn't

gives effective results in terms ofarea, delay and speed. Hence a new systemis proposed which is discussed in below section in detail manner.

PROPOSED SYSTEM

The proposed carry tree adder is utilized for performing the operation of addition. It is looking like structure of a tree for performing the arithmetic operation. Proposed carry tree adder is utilized for higher performance operation of addition. This adder contains Black cells and Graycells. Each Black cell contains two ANDgates and one OR gate. Multiplexer is a combinational circuit which contains multiple inputs and one output. Gray cell contains single AND gate only. Propagate is represented as P_n and this contains singleAND gate only which is given in below equation 1. Generate is denoted as G_n and this contains single AND gate and single ORgate which is denoted in below equation 2.

$P_n=B_n$ AND B_{n-1}----------(1)

$G_n=A_n$ OR [B_n AND A_{n-1}] (2)

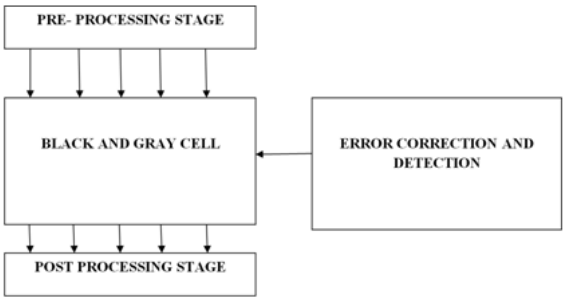

Fig. 2: BLOCK DIAGRAM OF PROPOSEDADDER

Proposed carry tree adder contains followingprimary stages, namely

1) Pre-computing
2) Carry Generation Network
3) Post-computing

1) Pre-computing stage: In this stage of calculation two signals such as Propagate and Generate are implemented using a pairof two input bits A and B. Propagate is the "XOR" function of two input bits and Generate uses "AND" function of two input bits. The Propagate (P_n) and Generate (G_n) are represented in following two equations 1& 2.

$P_n = A_n$ XOR B_n---------- (1)

$G_n = A_n$ AND B_n ----------(2)

2) Carry Generation Network: In this stage, the proposed adder differs from other PPA's in the structure. So, it forms the performance indicating stage of the adder. It contains the transforming elements and buffer elements. Less number oftransforming elements reduces the time delay. This stage generates carry for each bit which is known as Carry Generate (Cg). TheCarry Propagate and Carry Generate are used for another process which provides carry at final cell exist in each bit process. The final carry bit provides Sum output of the next bit simultaneously up to the finalbit. This carry is used for the next bit sum operation. The Carry Generate and Carry Propagate are represented in the following equations 4 & 5. The output of buffer element is same as that of input. The output of the transforming element is

$C_p = P_{i+1}$ AND P_i ---------- (3)

$C_g = G_{i+1}$ OR (P_{i+1} AND G_i) ---------- (4)

Where i = 0,1,2,3.....N. The Carry Propagate C_p in above equation 3 is known as Black cell and Carry

Generate C_g in above equation 4 is known as Gray cell.

3) Post computing stage: The sum output and the final carry output are evaluated in this stage. It is the final stage of novel

technique for addition. The carry output of an initial input bit is XORed with the next bit of Propagate which generates the sumoutput given in below equation 5.

$S_n=P_n$ XOR C_{n-1} ---------- (5)

REULTS

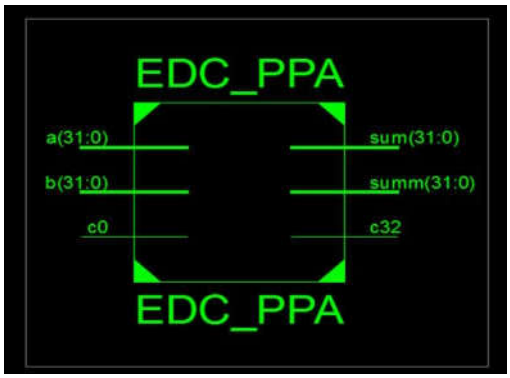

Fig. 3: RTL SCHEMATIC

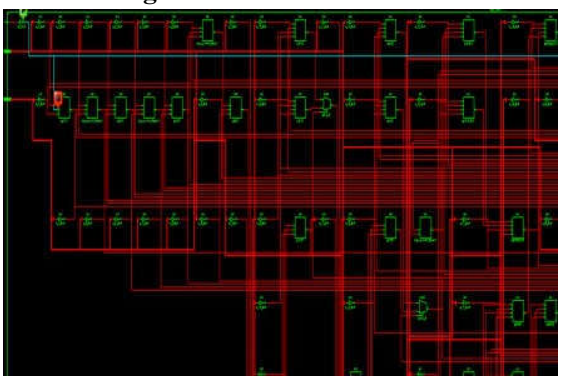

Fig. 4: TECHNOLOGY SCHEMATIC

Fig. 5: OUTPUT WAVEFORM

CONCLUSION

The research provides an approximation computing-based parallel adder design and implementation. CMOS and GDI techniques are only two of the design methodologies used to create the Parallel Adder. Performance of the variable latency adder mostly depends on the prefix-processing step. The quantity of black cells can be reduced with speculative latency adder. The designed parallel adder shows superior improvements in the variable latency in case of quick operation demand, in contrast to the traditional non-speculatively adders.

REFERENCES

[1] T. Yang, T. Ukezono, and T. Sato, “A Low-Power Configurable Adder for Approximate Applications”, 19thInternational Symposium on Quality Electronic Design, Mar. 2018.

[2] R. Ye, T. Wang, F. Yuan, R. Kumar, and Q. Xu, “On ReconfigurationOrientedApproximate Adder Design

and Its Application", IEEE/ACM International Conference on Computer-Aided Design (ICCAD), pp. 48-54, Nov. 2013.

[3] S. Venkataramani, V. K. Chippa, S. T. Chakradhar, K. Roy, and A. Raghunathan, "Quality programmable vector processors for approximate computing", 46th Annual IEEE/ACM International Symposium on Microarchitecture (MICRO), pp. 1-12, Dec. 2013.

[4] V. Gupta, D. Mohapatra, A. Raghunathan, and K. Roy, "Low-Power digital signal processing using approximate adders", IEEE Transactions on Comptuer-Aided Design of Integrated Circuits and Systems, vol. 32, no. 1, pp. 124-137, Jan. 2013

[5] J. Liang, J. Han, and F. Lombardi, "New metrics for the reliability of approximate andprobabilistic adders", IEEE Transactions on Computers, vol. 62, no. 9, pp. 1760-1771, Sep. 2012.

[6] R. Venkatesan, A. Agarwal, K. Roy, and A. Raghunathan, "MACACO: modeling andanalysis of circuits for approximate computing", IEEE/ACM International Conference on Computer-Aided Design (ICCAD), pp. 667-673, Nov. 2011.

[7] H. R. Mahdiani, A. Ahmadi, S. M. Fakhraie, and C. Lucas, "Bio-Inspired imprecise computational blocks for efficient VLSI implementation of Soft-Computing applications", IEEE Transactions on Circuits and Systems I: Regular papers, vol. 57, no.4, pp. 850-862, Apr. 2010.

[8] A. B. Kahng, and S. Kang, "Accuracy- configurable adder for approximatearithmetic designs", IEEE/ACM Design Automation Conference (DAC), pp. 820- 825, Jun. 2010

[9] M. S. Lau, K. V. Ling, and Y. C. Chu, "Energy-Aware probabilistic multiplier: Design and Analysis", International Conference on Compliers, architecture, and synthesis for embedded systems, pp. 281-290, Oct. 2009.

[10] V. Beiu, S. Aunet, J. Nyathi, R. R. Rydberg, and W. Ibrahim, "Serial Addition: Locally Connected Architectures", IEEE Transactions on Circuits and Systems-I: Regular papers, vol. 54, no. 11, pp. 2564-2579, Nov. 2007.

[11] S. Cotofana, C. Lageweg, and S. Vassiliadis, "Addition related arithmetic operations via controlled transport ofcharge", IEEE Transactions on Computers, vol. 54, no. 3, pp. 243-256, Mar. 2005.

[12] NanGate, Inc. NanGate FreePDK45Open Cell Library, http://www.nangate.com/?page_id=2325, 2008.