AN EFFECTIVE PLANNING AND CREATION OF A MULTILOOP CONTROLLER FOR FAST TRANSIENT DC-DC CONVERTERS

[1]LENKALA PRAVEEN KUMAR, [2]MITTAKANTI VINOD KUMAR, [3]MANCHIKATLA RANJITH KUMAR, [4]SRIRAMOJU MANILAHARI
[1, 2,3]Assistant Professor, [4]Student, Dept. of Electronics and Communication Engineering, Brilliant Institute of Engineering and Technology, Hyderabad, Telangana, India

ABSTRACT
A unique AC coupled feedback (ACCF) design is developed to achieve quick transient response while inherently managing the DC–DC switching converter's start-up in-rush current. Furthermore, the ACCF circuit aids in managing the output voltage's ramping speed during power-up, obviating the need for a bulky soft-start circuit. The new controller is straightforward to implement and takes up very little space on the chip. Using the CMOS technology, a buck converter with the suggested architecture was manufactured with an active silicon area of 0.6 mm2. The output voltage rises linearly during a soft-start period of 1.05 ms, as measured, conforming to the designed slope. The proposed ACCF is modified from a conventional capacitor multiplier and connected between the outputs of the converter and the transconductance. With this supplemental feedback, the transient response has been significantly improved due to the gain-boosting effect around the compensator's midband. Excellent load transient responses are achieved under different load current steps; the output voltage overshoot/undershoot of 60 mV settles down within 10 μs for a load variation from 50 μA to 1 A in 1 μs. Moreover, the proposed converter maintains both excellent load and line regulations of 0.019 mV/mA and 0.0055 mV/mV, respectively.

Enhancement of This Project:
Design of fast transient DC-DC convertor implemented in 45nm CMOS technology, and vary input voltage 2.6V ~ 4.2V.

1. INTRODUCTION

Step-down method of DC -to-DC power converter it is called Buck Converter. The operation of electromechanical device of DC-DC converter is converts direct current (DC) from certain level of input voltage to another voltage level. This paper proposes the novel design implementation of fast transient response current-mode buck converter with ac coupled feedback (ACCF). Where, ACCF is the modified design of a conventional Capacitor multiplier. The previous method of DC to DC Converters requires more power to achieve the fast transient to voltage conversion and it has high electromagnetic interface (EMI) noise. To overcome this problem this work presents a novel design of DC-DC converter with ACCF. ACCF circuit used to eliminate the bulky soft-start circuit when the ramping speeds of the output voltage during power-up. A Present Proposed system uses current mode- controller to improve response in speed and also increasing load transient voltages. The proposed scheme has been implemented in input voltage 2.6V ~ 4.2V and 45nm CMOS technology and compared in terms of Voltage, power, area and delay of the DC-DC converter will be calculated.

2. EXISTING SYSTEM

THE demand for fast load transient performance has grown significantly, affecting the power supplies of modern high-speed processors—especially processors targeting to achieve a fast transition from the low-power idle mode to the high-speed active mode. There is a massive load current change when the system switches from an idle mode to an active mode. Ideally, the regulator should maintain a voltage level that is almost constant, which means that there should be a negligible output voltage overshoot /undershoot and rapid response time. To accomplish these stringent requirements, various research works on fast transient dc–dc converters have been proposed.

The pole and zero are moved back immediately after the transient event to stabilize the system. However, a careful design targeting system stability during the whole process needs to be taken into consideration once the bandwidth is tentatively changed. Another commonly used method to improve the transient response is to increase of the slew rate of the error amplifier.

Among these methods, the increase of system bandwidth has been the most general solution for the majority of the analog circuits designed according to the linear control theory. In the design of a switching mode dc–dc converter, the wide system bandwidth can be achieved by adopting the current-mode control method. On top of that, an adaptive pole–zero position circuit has been proposed to instantly move the pole and zero pair of the compensation network to higher frequencies, in order to temporarily extend the bandwidth of the system during the transient event.

Different current-boosting modules are used to increase the source/sink current at the output of the error amplifier during the transient period. The required boosting current must be large enough to realize an obvious improvement on the transient response, and at the same time, it needs to avoid the over-response oscillation caused by the excessive boosting current. Moreover, current-boosting modules introduce more power consumption, which degrades the overall efficiency.

Besides that, the use of nonlinear control is an alternative to realize fast transient response. For example, hysteresis control can offer immediate feedback during load variations. However, this method has a drawback—the high electromagnetic interference (EMI) noise due to its variable switching frequencies. Circuits can be added to lock the switching frequency and thus abate the EMI noise, but such additions bring more complexities into the circuit design.

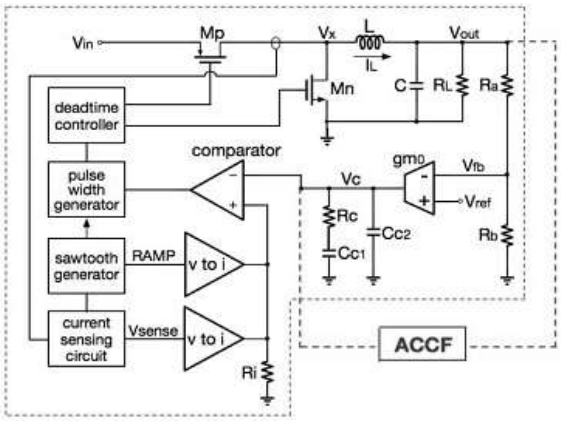


Figure 1: Conventional current-mode buck converter with the proposed ACCF loop

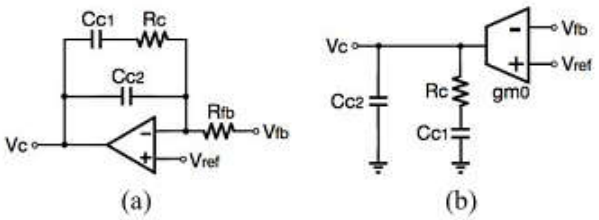


Figure 2: Type-II compensation designs. (a) OpAmp–RC topology. (b) Gm–C topology

The conventional current-mode buck dc–dc converter is highlighted with the blue dashed line. Differing from the conventional type-III compensation network which contains three poles and two zeros to boost the phase to ensure stability, the proposed method generates the same number of poles and zeros to boost the mid-band gain to significantly enhance the response strength of the compensator, thus increasing the transient response. At the same time, the proposed scheme also helps to manage the output voltage ramping speed during the converter power-up.

Theoretically, the transient performance depends mainly on two factors—the response speed and the response strength. The former can be interpreted as the delay time from the load transient event to the change on the control signal, and the latter refers to the amount of the amplitude changes on the control signal.

Taking the widely used type-II compensation design as an example here, the structure of the type-II compensation designs can be realized by either the operational amplifier–resistor–capacitor (OpAmp–RC) topology [as shown in Fig. 2(a)] or the transconductance–capacitor (Gm–C) topology [as shown in Fig. 2(b)]. During the load step, the variation in the output voltage results in a change in the feedback signalVfb. The control signal Vc can only respond gradually, due to the compensator's integrating effect. Its response speed depends on the bandwidth of the compensator. Assuming an error voltage Verr turns up on the feedback, the amount of change of the control signal (|Vc|) from its steady-state level can be expressed in the following equations for the

OpAmp–RC and Gm–C topologies, respectively [1]: $OpAmp--RC: Vc = Rc\ Rfb\ Verr$ …….(1)

$Gm--C: Vc = gm0RcVerr$ …….(2)

where Verr stands for the error voltage that turns up on the feedback, gm0 is the transconductance of the gm0 cell, and Rfb and Rc are the resistors connected to the inverting input terminal of the OpAmp and the compensation resistor, respectively.

3. DISADVANTAGES

- Difficult to achieve fast load transient performance.
- Current boosting modules in existing system require more power, which degrades the overall efficiency.
- High electromagnetic interface (EMI) noise.

4. PROPOSED SYSTEM

This paper utilizes a current-mode controller to improve the response speed aspect by increasing the system bandwidth in order to enhance the load transient response. On top of that, a novel ACCF is paralleled around the compensator to boost the response strength at the mid-band (as shown in Fig. 3), which is lacking in the conventional designs. The output impedances of both gm0 cell and ACCF are assumed to be infinity (which will be discussed in Section III). The transfer function of the conventional type-II compensation network can be expressed in (3) which includes two poles and one zero (located at p1, p2, and z1, respectively). With the additional ACCF, three poles and two zeros will be generated (located at p 1, p 2, p 3,z 1, and z 2, respectively), and the newly generated poles and zeros will boost the compensation mid-band gain as derived in (4). The respective Bode plot can be found in Fig. 4 accordingly

Without ACCF:

$$\frac{v_c(s)}{v_{out}(s)} = \frac{\alpha(s-z1)}{(s-p1)(s-p2)}$$

$$z1 = \frac{1}{2\pi\, Rc1Cc1}$$

$$p1 = 0$$

$$p2 = \frac{1}{2\pi\, Rc1Cc2} \qquad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (3)$$

$Wit ACCF$:

$$\frac{v_c(s)}{v_{out}(s)} = \frac{\alpha'(s-z1')(s-z2')}{(s-p1')(s-p2')(s-p3')} \qquad \ldots\ldots\ldots\ldots\ldots\ldots (4)$$

$were$

$$vc(s) = (i1 + i2)\frac{1 + RcCc1s}{s(Cc1 + Cc2)\left(Rc\frac{Cc1Cc2}{Cc1+Cc2}s + 1\right)}$$

$$1 = -gm0\frac{Rb}{Ra + Rb}Vout$$

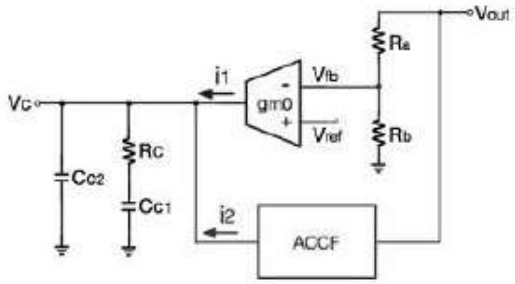


Figure 3: Proposed compensation network

where i1 and i2 are the output current from the gm0 cell and ACCF, respectively, α and α are constant coefficients, Ra and Rb are the voltage divider series resistors connected at the output of the dc–dc converter, and Cc1, Cc2, and Rc are the compensation capacitors and resistor, as shown in Fig. 3. Furthermore, the ACCF circuit also defines the output voltage rising slope during the converter power-up. The working principle of the soft-start function is illustrated in Fig. 5. During start-up, Vout is much lower than Vref, so that the gm0 cell will be saturated with an extremely high output voltage Vc, which will program an unfavorable runaway inductor current. With the help of the ACCF circuit, in this case, the fast-rising voltage appearing at Vout caused by the inrush start-up current is coupled through the ACCF and induces the ac current from Vc into the ACCF itself. As a result, Vc is pulled down to define the slow increase in the inductor current and output voltage. This particular inherent function of the proposed ACCF eliminates the need for a dedicated soft-start circuit in the conventional designs.

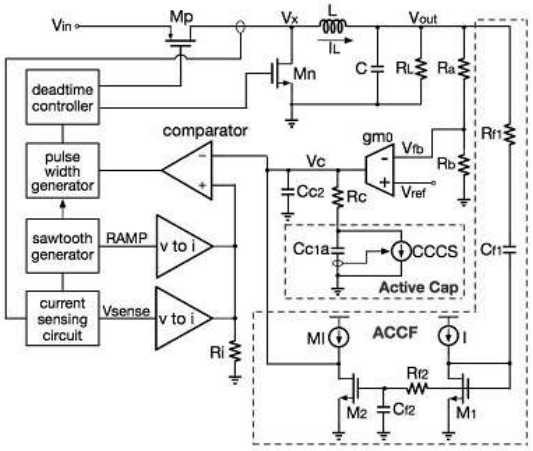
5. CIRCUIT IMPLEMENTATION

A. Active Compensation Capacitor

Active capacitor has been proposed and used in the amplifier to amplify capacitance in [21]. In this paper, the large passive compensation on-chip capacitor Cc1 is replaced by the equivalent active capacitor in the proposed buck converter to reduce the footprint, as shown in Fig. 6. The schematic of the active capacitor will be also modified and used in realizing the ACCF, which will be discussed later. Equations (5)–(7) explain the derivation of the equivalent active capacitor from the passive capacitor mathematically. The equivalent circuit of (7) is modeled in Fig. 6(b) as an active capacitor. The current mirror is used as the current control current source to amplify the ac current in this work. Fig. 7 shows the circuit implementation of the active capacitor by using the current mirror. A (N + 1) times smaller passive capacitor is utilized in parallel with the current mirror, which has an amplification factor of N (N = 19 in this paper), to realize the same capacitance as Cc1(Cc1 = 80 pF in this paper). Fig. 8 shows an approximately seven-time-reduction in the silicon area with the use of the equivalent active capacitor. The higher the value of N, the smaller is the footprint of the active capacitor.

B. Multiloop Control for Transient Enhancement and Soft-Start

The main structure of the ACCF circuit is modified from the active capacitor circuit , where an ordinary on-chip capacitor C f 1 is ac coupled from Vout, amplified by the current mirror (transistor M2-to-M1 with the ratio M:1, M > 1), and connected back to the main control loop at the gm0 cell output node, as shown in Fig. 9. The circuit implementation of the gm0 cell is shown in Fig. 10. Resistor Rgm is inserted in between the source terminals of MP1 and MP2 to sense the voltage differences (V) between the input terminals (V+ and V−) of the two super-source-followers;



hence, gm0 of the cell will be inversely proportional to the value of Rgm . The output current is generated by the two pairs of current mirrors formed by MP3, MP4, MN3, and MN4 at the output stage, and it will charge the compensation network at the output of the gm0 cell. The mid-band gain (Amid-band) of the gm0 cell is, therefore, proportional to Rc while inversely proportional to Rgm , as expressed in (8). Eventually, the process, voltage and temperature variations of the two resistors are effectively canceled. Nevertheless, Rc should be placed close to Rgm in the layout for a better matching purpose.

1) **Soft-Start Analysis**: With the help of the ACCF, the fast rising voltage appearing at Vout caused by the start-up in-rush current will be coupled through C f 1. Then, an ac current will be inducted into the transistor M1. The M2-to-M1 current mirror is able to amplify the induced current and pull it from Vc; therefore, Vc is adjusted to a lower level. Consequently, Vc, inductor current, and Vout are well managed by the current control loop.
2) **Steady-State Analysis**: The ACCF path is virtually disconnected from Vout during the steady state. The low pass filter R f 2C f 2 is added to prevent the Vout ripples from passing through the ACCF path and disturbing Vc. It is designed to cut off around the converter's switching frequency. Although there is no current flowing between the gm0 cell and the ACCF circuit, the output impedance of the gm0 cell is reduced due to the ACCF output stage. The advanced current mirror with high output impedance should be considered on condition that a large dc loop gain is preferred.
3) **Transient Analysis**: As discussed previously, the load transient performance is improved on account of the gain boosting effect around the compensator's mid-band. This can be understood analytically by deriving the transfer function from the small-signal equivalent circuit, as shown in Fig. 11(a). The transconductance of the transistors M1 and M2 are labeled as gm1 and gm2 (gm2 = Mgm1), and RO represents the combined output impedances of the gm0 cell and the ACCF. The original single-loop compensation capacitor Cc1 still determines the dominant pole in this multiloop network.

C. Continuous-Sensing-Technique for Fast-Response Current Sensor

The current sensor has been used to sense the inductor current in the current-mode dc–dc converter. The conventional design is shown, where a sense FET (SenFET) is implemented to sense the current passing through the high side power FET MP at the ratio of k to 1

6. AN AC COUPLED FEEDBACK CAPACITOR

An AC coupled feedback (ACCF) is introduced using a capacitor multiplier from the output of the converter to the output of the error amplifier. With this additional feedback, the transient response, which used to be limited by the compensator mid-band gain has been significantly improved. Meanwhile, the ACCF circuit can help to control the converter output ramping speed during power-up, thus eliminating the bulky soft-start circuit. The simplified circuit design means the new controller can be realised by a tiny on-chip circuit.

The APZP technique triggers the two-step nonlinear control mechanism to speed up the transient response at the beginning of load variations. Before the output voltage is regulated back to its voltage level, the APZP

technique merely functions as a linear control method to regulate output voltage in order to ensure the stability of the system.

The overshoot/undershoot voltage and the transient recovery time are effectively reduced. The APM control can always maintain the system phase margin at an adequate value under different load conditions. That is, the compensation pole-zero pair is adapted to load current to extend the system bandwidth and get an adequate phase margin.

A monolithic current-mode CMOS DC-DC converter with integrated power switches and a novel on-chip current sensor for feedback control is presented in this paper. With the proposed accurate on-chip current sensor, the sensed inductor current, combined with the internal ramp signal, can be used for current-mode DC-DC converter feedback control. In addition, no external components and no extra I/O pins are needed for the current-mode controller.

An integrated current-sensing circuit for low-voltage buck regulator is presented. The minimum achievable supply voltage of the proposed current-sensing circuit is 1.2 V implemented in a CMOS technology with V/sub TH/=0.85 V, and the current-sensing accuracy is higher than 94%.

The advantages and limitations of the existing conventional techniques are discussed and analyzed. With the proposed SDP technique, a nearly optimized recovery time speedup and voltage drop minimization for every different conventional current-mode converters can be obtained.

CONCLUSION

The proportional compensator in the proposed converter, there is no need of external compensation components in this design. As a result, a compact-size and high-performance dc-dc buck converter can be guaranteed. Experimental results show that load regulation can be improved from 0.5 to 0.025 mV/mA.

To save power consumption in steady state, the accelerative mechanism of the EA is turned off. A buck converter with CBM is implemented with 0.35 μm 2P4M complementary metal-oxide-semiconductor process. The experimental results demonstrate that the recovery time and transient ripple of the buck converter are improved by over ten times and two times, respectively, compared with those of the buck converter without CBM, for a 450 mA load current change.

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