# Bridging the gap between converters and multiple SMPS output using the PEC method to improve power quality

## <sup>1</sup>K.LAVANYA, <sup>2</sup>K.CHANDRA REDDY, <sup>3</sup>L.NADAM, <sup>4</sup>RATHLAVATH YUVARAJ

<sup>1, 2,3</sup>Assistant Professor, <sup>4</sup>Student, Dept. of Electrical and Electronics Engineering, Brilliant Institute of Engineering and Technology, Hyderabad, Telangana, India

### ABSTRACT

A power-factor-correction (PFC) multiple output switched-mode power supply (SMPS) with a bridgeless buckboost converter at the front end was designed, analyzed, and developed. To eliminate the diode bridge rectifier, a single-phase ac supply is routed to a pair of back-to-back linked buck-boost converters, resulting in lower conduction losses and improved power quality at the front end. By simulating this circuit in the MATLAB/Simulink environment, and the findings acquired through simulation, the operation of the bridgeless buck-boost converter in discontinuous conduction mode provides inherent PFC operation and lowers complexity in control under fluctuating input voltages and loads. Our simulation findings show that the suggested SMPS has better performance.

Keywords: SMPS, PFC, Power quality, Buck-boost converters.

#### 1. INTRODUCTION

Switched-Mode power supplies (SMPSs) are used for powering up different parts in a personalcomputer (PC) by developing multiple dcvoltages from a single-phase ac voltage from the power grid. Normally, a diode bridge rectifier (DBR) followed by a filter capacitor is used at the front end of these SMPSs.DBR causes significant deterioration in the power quality leading to very low powerfactor (PF) and high harmonic distortion at the ac mains with a high crest factor of the input current Fig. 1.a shows the input voltage and input current of a typical SMPS that is currently employed in most of the PCs. The current waveform is very peaky, non sinusoidal, and highly distorted; the PF is around 0.48. At full load, the total harmonic distortion (THD) of input ac mains current is 83.5%.

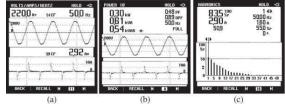


Fig. 1. (a) Conventional SMPS input voltage and input current, (b) input power and PF, and (c) inputcurrent harmonic spectrum

The performance of the power supply is violating the limits set by various international standards such as the International Electro technical Commission (IEC) 61000 -3-2 Due to these issues, improved-power-quality SMPSs are extensively being researched, which are expected to draw a sinusoidal input current at a high PF. Improvement in power quality also results in better reliability and enhanced efficiency. To achieve a perceivable improvement in power quality, PF correction (PFC) circuits are employed in these SMPSs at the utility interface point PFC circuits are able to achieve high PF andlow THD in the input current even at fluctuating input voltages and varying loads.

Apart from this, they are also capable of yielding stiffly regulated output dc voltages. The use of non isolated PFC converters at the front end of these power supplies is a commonly accepted solution to achieve a good power quality at varying input voltages and loads Discontinuous

conduction mode (DCM) operation of these converters results in inherent PFC and reduction in sensor requirements. Furthermore, DCM can also be implemented with simple control strategy. Recent advancements in the field of powerelectronics have enabled the elimination of DBR at the front end of the power supplies, thereby improving the power quality at the ac mains. Various bridgeless single endedprimary-inductance converter and Cuk converters are proposed in the literature, which result in low voltage stress, improved thermal management, and low conductionlosses .However, the component count is increased in these converters, which is not suitable for low-power SMPS applications, although the output voltage range is fairly large. A bridgeless buck PFC converter is proposed in which acts as a voltage doubles. A bridgeless boost converter is reported in which eliminates one diode drop in the current path. However, in both converter topologies, the output voltage range is limited. A buck-boost converter configuration is best suited for computer SMPSs among various bridgeless converter topologies particularly because it can handle a larger voltage range and yet deliver stiffly regulated output voltages. Such a bridgeless buck-boost converter is proposed for niverse input PFC applications, which offers low switch stress, reduced magnetic size, and low inductor conduction losses. However, one of the switching devices isalways on in the conduction path. Wei et al. have proposed a bridgeless buck-boost converter that uses three switches in the conduction path, which increases the conduction losses.

Normally, a half-bridge voltage source inverter (VSI) is used at the output for high-frequency isolation and multiple dc output voltages in computer power supplies because it provides better core utilization than any other unipolar converter and it is cost effective compared to push–pull and full-bridge converters. It is observed from the available literature that the bridgeless converter- based multiple-output SMPS has not been attempted so far, particularly targeting SMPSs for PCs. Therefore, an attempt is made here to reduce the current harmonics and to achieve high PF at theutility interface in a multiple-output SMPS by using a bridgeless buck–boost converter at the front end. The diode bridge at the front end is eliminated, and two buck–boost converters are connected back-to-back so that each takes care of one half cycle of the ac supply. The bridgeless buck–boost converter is designed in DCM for single control loop and for inherent PFC.

This regulated dc voltage is given to half-bridge VSI for obtaining multiple- output dc voltages. The half-bridge VSI is designed in continuous conduction mode to reduce the component stress. Moreover, only one control loop is required to regulate multiple dc voltages. The proposed system is designed, analyzed, and simulated in MATLAB/Simulink software, and the performance is studied during varying input voltages and loads to demonstrate the improved performance in terms of low THDand high PF. The hardware of the proposed SMPS system is developed as an experimental prototype, and the simulated results are validated with the help of test results on the prototype to confirm the improved power quality at the ac mains.

### 2. PROPOSED CONCEPT

The proposed computer power supply consists of mainly two parts, bridgeless front end ac-dc converter and multi output isolated dc-dc converter. The front end converter is designed in discontinuous conduction mode (DCM) for achieving inherent PFC while the isolated converter is designed in continuous conduction mode (CCM). The control loops of both converters are independent of each other. The system configuration and operating principle of the SMPS system has been described in the following subsections.

### 3. SYSTEM CONFIGURATION

The configuration of proposed power supply with four regulated dc output voltages is shown in Fig.2.1. At the input side, DBR is eliminated by using two SEPICs. The upper converter operates in the positive half cycle and the lower one in the negative half cycle of the input ac voltage. The switching frequency of both the converters is set at 20 kHz for efficient control. The design of output inductors for both the converters is carried out in DCM to reduce the complexity in control. The regulation of the output voltage is able to take care of wide variations in the input voltage and load. The output dc voltage is sensed and compared with a reference voltage from which

the voltage error is obtained which is given to a proportional and integral (PI) controller; the PI controller output is compared with a high frequency saw-tooth wave to yield PWM pulses that are given to both switches simultaneously. The width of these PWMpulses varies according to the output of the PI controller so that the output dc voltage is regulated effectively which is, in turn, fed tothe isolated half bridge converter in the second stage to obtain multiple isolated regulated output voltages. The isolation iseffected through multi-winding high frequency transformer (HFT). A centre tapped configuration is chosen at the output side to reduce the conduction losses. All the secondary windings are controlled via one control loop. The highest rated secondary winding of the HFT is selected for voltage sensing. The difference between the output voltage and reference voltage is fed to another PI controller whose output is compared with another high frequency saw- tooth wave to generate second set of PWM signals for the half-bridge converter devices S1 and S2. Care should be taken to make sure that there is sufficient dead-time between turning OFF of S1 and turn-ON of S2 to avoid shootthrough. The isolated converter is operated in CCM to take the advantage of reduced stress. If the load in any of the winding changes, the duty cycle changes accordingly to ensure regulated dc outputs. The response of the other outputs is slower than the one where the output voltage sensed.

#### 4. OPERATING PRINCIPLE

The operation of the front end converters and the isolated converter are described independently as follows:

#### **OPERATING PRINCIPLE OF THE FRONT ENDCONVERTER**

During the positive half cycle of the input voltage, the upper SEPIC operates as shown in Fig.2.2. In the same way, during negative half cycle the lower SEPIC would operate. The operation of the SEPIC in one PWM cycle is described with the help of the following modes: In the first mode, the high frequency switch  $S_p$  turns on, the input inductor Lp1 starts storing the energy which is transferred from the single phase ac mains as shown in Fig.2.3a. Diode  $D_{p1}$  completes the current path. In the second mode,  $S_p$  is turned off and diode  $D_{p2}$  starts conducting. The energy in output inductor  $L_{p2}$  starts decreasing to zero which is shown in Fig.2.3b. In the last switching state, the current in the output inductor remains zero until the start of next switching cycle. This mode ensures the DCM operation as shown in Fig.2.3c.

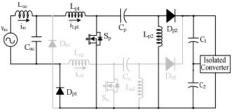


Fig.2.2 Operation of PFC converter when he input voltage is positive

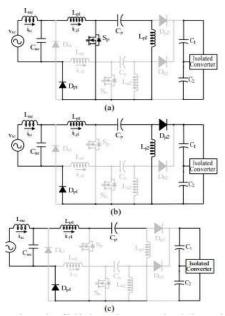


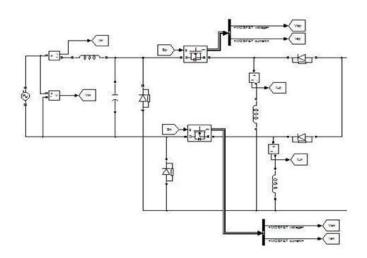
Fig.2.3 Operating modes of bridgeless PFC converterwhen the input voltage is positive

#### **OPERATING PRINCIPLE OF ISOLATEDCONVERTER**

Two high frequency switches are turned on and off alternately in one switching cycle. So, the operation of the converter in one half of the switching cycle is the same as that of the other half cycle. In the first half cycle, the upper switch  $S_1$  is turned on. The diodeson the secondary side start conducting and the inductors in all the secondary windingsstart storing energy. All the filter capacitors

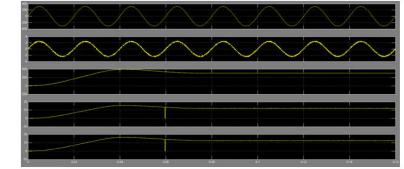
#### 5. SIMULATION RESULTS: SIMULINK DIAGRAM

discharge through the loads to maintain dc output voltages as constants. In the next half cycle of the PWM period, the upper switch is turned off. The secondary diodes are turned on to free-wheel the inductors currents. The current in the all the secondarywindings cancel the core flux so that the net voltage across the HFT becomes zero.



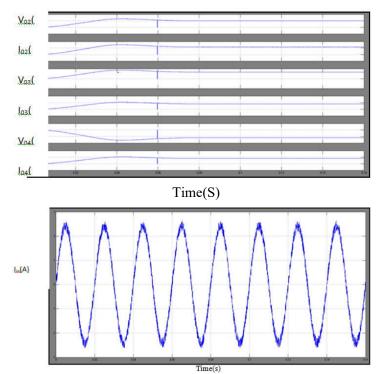
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#### BUCK BOOST CONVERTER

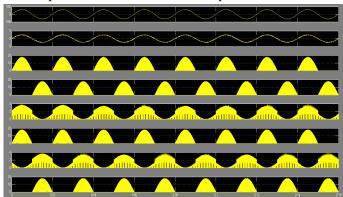


Time(S)

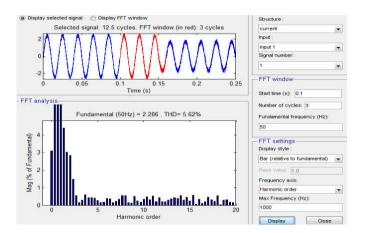
Input voltage current, buck-boost converter output voltage, half bridge VSI output voltages, and current at 220v and full load.



Input voltage current, buck-boost converter output voltage, half bridge VSI output voltages, and Time(s) Waveform of input current and its harmonic spectrum at 220v and full load



waveforms of  $v_{in},\!i_{in},\!i_{Lp},\!i_{Ln},\!V_{Sp},\!I_{Sp},\!V_{Sn}$  and  $I_{Sn}$  at 220v and full load.



## CONCLUSION

bridgeless-converter-based multiple-output SMPS has been simulated and implemented to demonstrate its capability to improve the power quality at the utility interface. The output dc voltage of the first-stage buck–boost converter hasbeen maintained constant, independent of the changes in the input voltage and the load, and it is operated in DCM to achieve inherent PFC at the single-phase ac mains.

A satisfactory performance has been achieved during varying input voltages and loads with power quality indices remaining within the acceptable limits set by IEC 61000-3-2. Finally, a prototype of the proposed bridgeless-converter based multiple-output SMPS has been developed to validate its performance experimentally. The proposed SMPS has shown satisfactory performance, and hence, it can be recommended as a tangible solution forcomputers and other similar appliances.

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