4-Bit ALU Design using CMOS & GDI Techniques

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Abstract— In this paper, the design of an 4-bit Arithmetic Logic Unit (ALU) using Gate Diffusion Input (GDI) technique is proposed. Implementing the GDI technique in designing the ALU results in low power consumption and the number of transistors it requires is much less. Which result in reduced chip-area and power consumption – two of the most important parameters in digital VLSI design. In this design, XOR is used in the full adder. Moreover, a novel 1-to-4 demultiplexer circuit has been used in the design as well. A considerable number of research papers are studied and compared various logic families and then finally designed an 4-bit ALU which can perform 4 different operations. The design is validated using the schematic editor- and the simulation have been carried out using Mentor Graphics.

Keywords—ALU, GDI, CMOS, VLSI Design, XOR, Adder, Mentor Graphics

I. INTRODUCTION

The main part of a Central Processing Unit (CPU) is the Arithmetic Logic Unit (ALU) [1] which performs all kinds of arithmetic operations like addition, subtraction, multiplication, division and logical operations such as Inversion, ORing, ANDing, XORing, Multiplexing and other Boolean operations. Any device capable of processing needs an ALU- be it a VLSI chip or application specific smaller circuits. Improving the design of the ALU results in substantial improvement in the power requirements and overall performance of the entire processor.

Compact implementation and low power dissipation are the basic objectives in designing larger and complicated circuits, ALUs are no exception. A lot of effort has been given over the past few decades to make conventional CMOS based circuits more compact and power-efficient [2-4]. Subsequently, Domino Logic, pass Transistor Logic, Double Pass Transistor Logic, Transmission Gate Logic and many other techniques have been developed and implemented to enhance the performance of CMOS based circuits [5-7].

There are only two transistors in a basic GDI cell - an NMOS and a PMOS. It has four terminals- G, N, P and D; the first three act as input terminals [9]. But, a major issue with GDI technique is that it has swing problem [10]. It happens because the NMOS produces a weak logic 1 and the PMOS produces a weak logic 0. This problem is overcome by bringing about some modifications to the existing GDI technique. The modified GDI technique turns out to be more efficient than PTL and CMOS [12].

Similarly, the CMOS magnitude comparator requires 66 transistors whereas the GDI equivalent requires only 30 [17].The major segments of the proposed m-GDI ALU are:-

- ***Arithmetic Unit:* -** This unit performs basic arithmetic operations- like, addition and subtraction.
- ***Logical Unit:* -** This unit carries out logical operations. This paper presents OR, AND, XOR, NOT, NAND gates.
- A buffer unit has been used to select the desired input line.

EXISTING METHOD

It is a replacement technique of low-power digital combinatorial circuit style is delineated. This system permits reducing power consumption, propagation delay, and space of digital circuits whereas maintaining low complexness of logic style. Performance comparison with ancient CMOS and numerous pass-transistor logic style techniques is conferred. The various ways area unit compared with regard to the layoutspace, variety of devices, delay, and power dissipation.

Proposed Method

Gate Diffusion Input or GDI technique is a new method for designing circuits which reduces the power requirements considerably [4]. Also, GDI results in a reduced number of transistors, which in turn makes for a decrease in chip-area giving an edge to the designs over conventional methods [9].

The basic GDI primitive cell is similar to the CMOS implementation of the inverter circuit [13]. But, it is capable of doing much more than that. Depending on the inputs given to G, N and P the functionality of the circuit varies. G is the common gate of the NMOS and PMOS.

The primitive GDI cell itself can perform a number of functions. The inputs and the outputs have been presented in a tabular format in TABLE I.

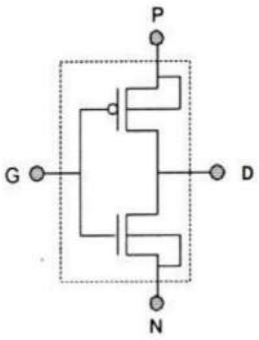


Fig. 1: A Basic GDI primitive cell

TABLE I: FUCTIONALITIES OF THE PRIMITIVE CELL

P	N	G	Output	Function
1	0	A	A’	NOT
0	B	A	AB	AND
B	1	A	A+B	OR
B	0	A	A’B	Function 1
1	B	A	A’+B	Function 2
A	B	S	AS+ BS’	2:1 MUX
A	B’	B	A’B+ AB’	XOR
A	B	B’	AB+ A’B’	XNOR

The biggest problem is the difficulty in fabrication using existing CMOS technologies [15]. As mentioned earlier there is the problem of swing degradation as well.

To overcome these problems, a modified version of the GDI cell has been proposed.

In the modified GDI cell the balk terminals of the PMOS and the NMOS are connected to VDD and ground respectively

In the ALU developed some of the logical circuits have been designed using the GDI technique .

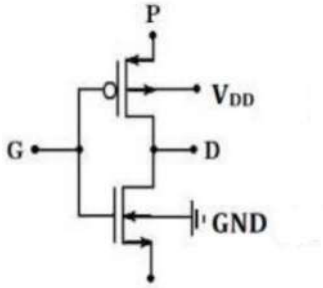


Fig. 2: A Basic GDI primitive cell.

II. 3T XOR

Using GDI the XOR gate can be implemented employing only three transistors as shown in [12-14], one less than what it takes to implement it using GDI. The 3T XOR design is given below in Fig. 3.

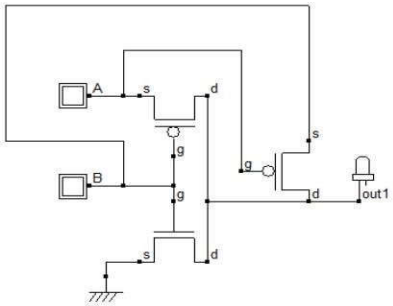


Fig. 3: The XOR design using GDI & CMOS

All the XOR gates used in the proposed ALU are XOR gates. This has resulted in a substantial decrease in the number of total transistors in the entire design and a reduction in the total power consumption.

One input (A) is fed to both the source and the gate terminals of PMOS, the other input (B) is fed to the common gate input terminal of both the PMOS and the NMOS as well as to the source terminal of the PMOS in order to implement the XOR. The common drain terminal of the transistors acts as the output terminal.

The resultant 3T XOR has a very small delay of 1 transistor only. But, it comes with the caveat that the output logic level may sometimes get skewed. However, Dan Wang et al has shown in [14] that by adjusting the W/L ratio the desired logic level at output can be ensured at all times.

The full adder [12] and full subtractor [13] designed using this 3T XOR are shown below in Fig. 4 and Fig. 5 respectively.

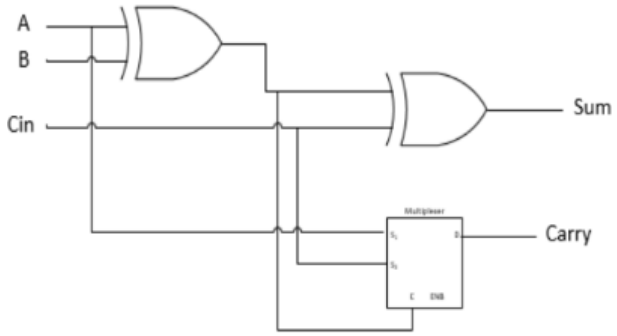


Fig. 4: 4T Full Adder

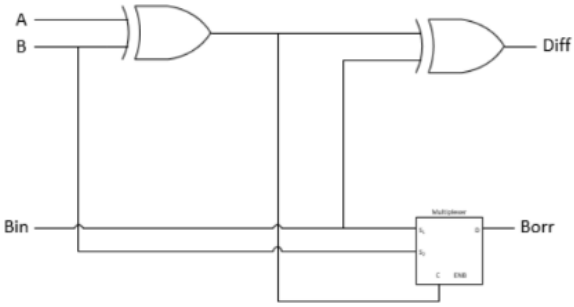


Fig. 5: 4T Full Subtractor

III. COMPONENTS OF THE PROPOSED ALU

AND, OR, NAND & NOT gates, MUX, comparator, buffer circuits have been implemented using GDI [4,13,17]. Diagrams of these circuits are given below from Fig. 6 to Fig. 11:

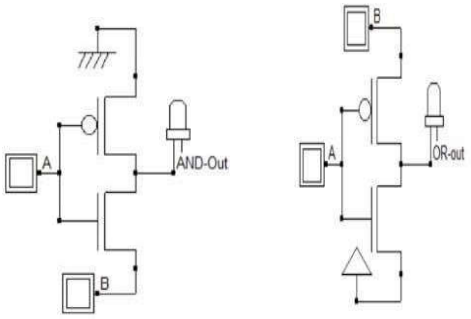


Fig. 6 : 2T AND & 2T OR using GDI

Selection of the desired input when necessary is facilitated by implementing a buffer circuit. The buffer circuit secures the output as well as adds a little delay which is desired while working with other large circuits. The buffer circuit has been illustrated in Fig. 11.

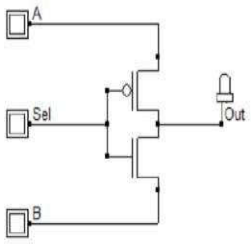


Fig. 7: 2T MUX using GDI

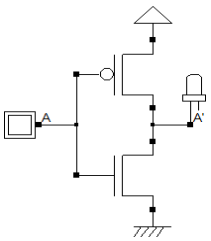


Fig. 4: 2T NOT using GDI

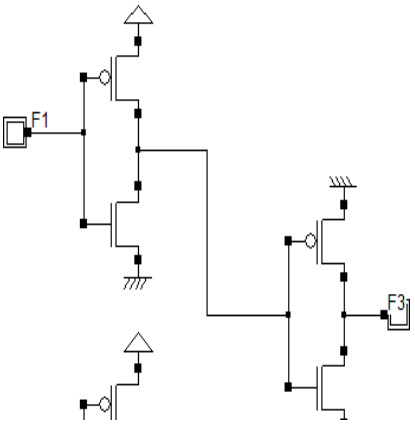


Fig. 9: Comparator using GDI

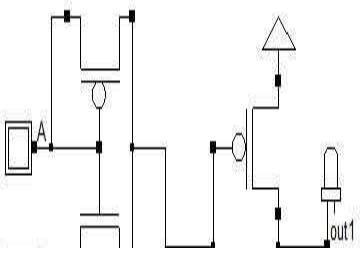


Fig. 10: NAND using GDI

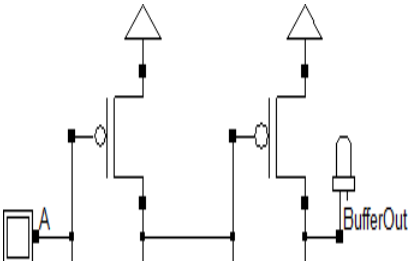


Fig. 11: Buffer Circuit

So far, all the basic blocks of the ALU have been covered, now it is equally important to incorporate a mechanism that would enable us to choose any one from all the logical and arithmetic modules. For this, taken a 1-to-4 demultiplexer which will work in tandem with sixteen sleep transistors (2 for each module) to choose and enable the desired circuitry.

The multiplexer design is a novel design, in that it has been designed using GDI cells. The circuit diagram is given below.

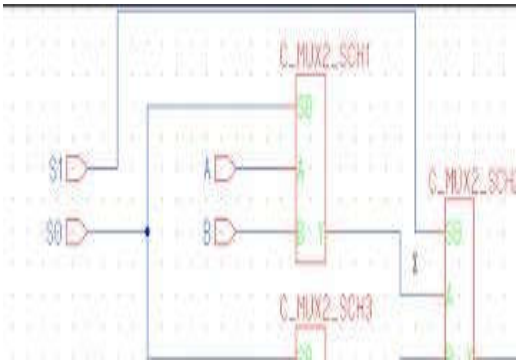


Fig. 12: 4*1 Multiplexer using GDI

The internal circuit diagram of the identical blocks used 14 times is given below. It is nothing but a simple 1-to-2 multiplexer implemented using GDI.

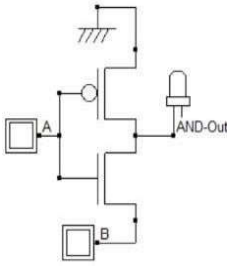


Fig. 13: 1:2 DEMUX using GDI

Wrapping up all these bits and pieces together got the complete ALU circuit as shown in Fig. 15. For the sake of convenience in demonstration, internal circuitry of vital modules has been replaced with blocks. However, detailed circuit diagrams of all the circuits have been given above.

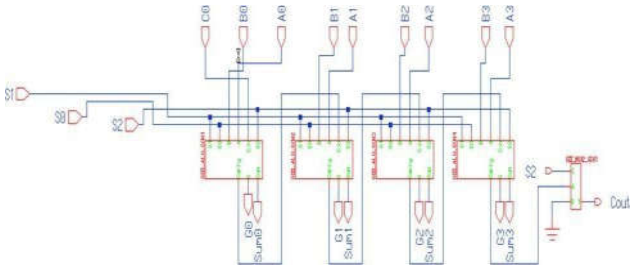


Fig. 15: The complete proposed 4-Bit ALU circuit

IV. RESULT & SIMULATION

The simulations have been carried out using DSCH 3.5, starting from transistor level design and further verified using Xilinx ISE 14.7 environment.

The simulation results of all the individual components realized using m-GDI, GDI and CMOS logic have been presented.

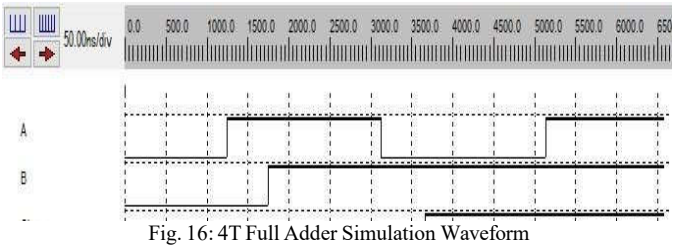


Fig. 16: 4T Full Adder Simulation Waveform

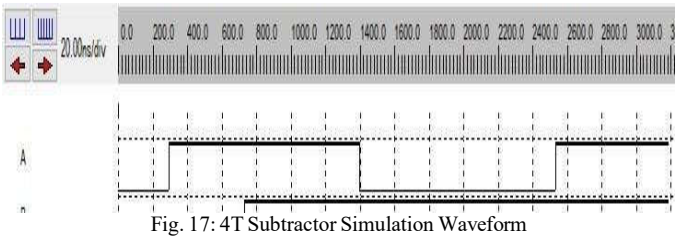


Fig. 17: 4T Subtractor Simulation Waveform

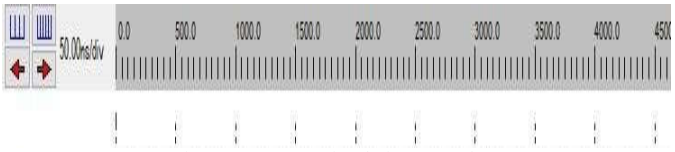
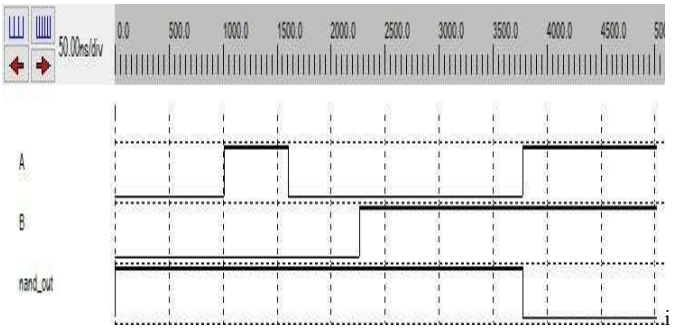


Fig. 14: 3T XOR Simulation Waveform



g. 19: NAND Simulation Waveform

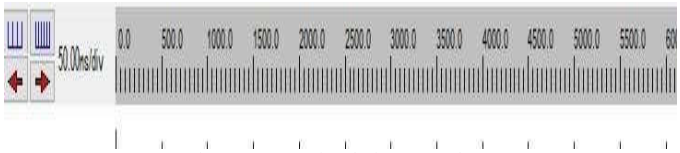


Fig. 20: AND Simulation Waveform

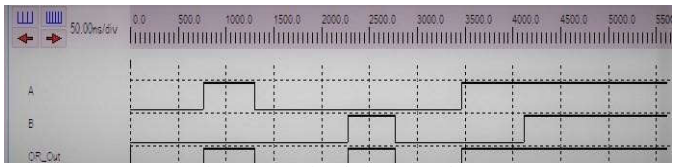


Fig. 21: OR Simulation Waveform

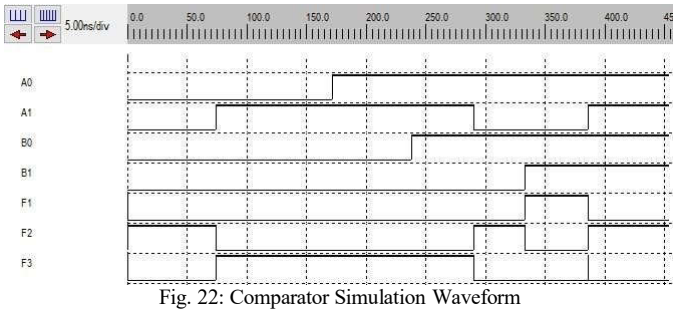


Fig. 22: Comparator Simulation Waveform

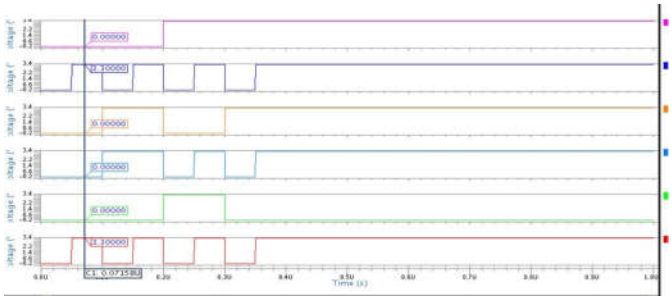


fig23:ALU Simulation-1

The simulation of the final ALU circuit as seen in Mentor Graphics is shown below.

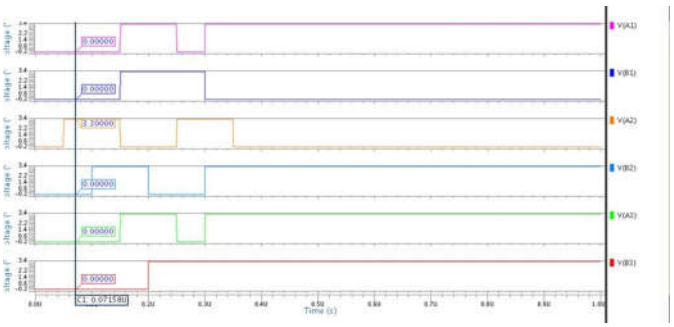


Fig. 25: ALU Simulation – II

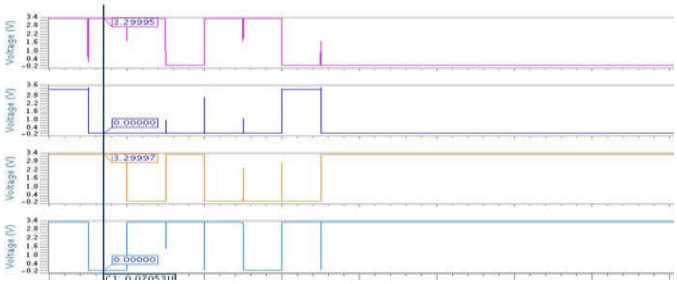


Fig. 26: ALU Simulation – II

V. CONCLUSION

Table II shows a comparative analysis of our proposed model with the other two models into consideration which have been discussed in [4] and [11].

TABLE II: COMPARITIVE ANALYSIS OF ALUS

Type of ALU (Design)	Power (uW)	DelayPath) – (ns)	Number of Transistors Required
4-bit ALU [4]	34.9	6.95	404
4-bit ALU CM OS [11]	43.4	6.01	745
Proposed Model	31.57	4.57	760

The table shows that the proposed ALU not only has the least number of transistors, but also, outperforms the rest in terms of power and critical path delay. Thus it is seen that the proposed model of GDI is more efficient compared to the conventional ones.

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